Recovery dynamics and fast (sub-50ns) read operation with Access Devices for 3D Crosspoint Memory based on Mixed-Ionic-Electronic-Conduction (MIEC)

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Abstract

BEOL-friendly Access Devices (AD) based on Cu-containing MIEC materials [1-4] are shown to be capable of both maintaining and moving rapidly between all the roles necessary for 3D crosspoint memory (*un-selected, half-selected, selected(read)*, and *selected(write)*). Ultra-low leakage is maintained over hours, recovery dynamics after both write (30-50uA) and read (3-6uA) operations are explored, and read operations fast enough for use with MRAM (sub-50ns) at low voltages are demonstrated.

Keywords: Access device, MIEC, PCM, NVM, RRAM, MRAM

Introduction

3D-stacking of large crosspoint arrays in the BEOL can allow a nonvolatile memory (NVM) to be as cost-effective as 2D NAND FLASH ($\leq 4F^2/3$). MIEC-based ADs exhibit the large ON/OFF ratios needed for such arrays (Fig. 1), with high voltage margin V_m (for which leakage is $\leq$10nA), ultra-low leakage (<10pA), high enough write currents (>100uA) even for PCM, and the bi-directional nonlinearity needed for stacking high-density MRAM and RRAM in the BEOL [1-4]. In addition, we have shown both scalability to <30nm CD and <15nm thickness [4], and tight distributions and 100% yield in large (512kBit) arrays [3].

In a crosspoint array, each AD must fill multiple roles: holding ultra-low (∼10pA) leakage at low *un-selected* bias for hours; maintaining modest (∼10nA) leakage at *half-selected* bias for seconds; and occasionally being *selected* to pass either read-level (3-6uA) or write-level (30-60uA) currents through its NVM (Fig. 2). The AD must maintain low leakage over very long periods, yet switch into a current-passing role and back to low leakage, quickly and seamlessly. To date, we have shown fast turn-ON speeds (15ns) of MIEC-based ADs, mostly in the PCM write regime (≥100uA) [4].

In this paper, we show that MIEC-based ADs maintain *half-* and *un-selected* states with ultra-low leakage over hours. We explore the time to recover low-leakage after both NVM-write (30-50uA) and NVM-read (3-6uA) operations, demonstrate fast NVM-reads (<50ns) suitable for MRAM, and show similarly fast turn-ON in thinner ADs with less overvoltage (thus minimal read disturb).

Stability of low-leakage in MIEC ADs

MIEC-based ADs are integrated on 8" wafers, using sputter-deposition of Cu-containing MIEC material into vias followed by an optimized CMP process [2] and a confined, non-ionizable TEC. Small "1T-1AD" device arrays are integrated with 180nm-node FETs (Fig. 3(a)) [2-4]; "short-loop" devices (Fig. 3(b)) are tested with Conductive-AFM [3-4], using a proximate bottom contact with low series resistance made by removing nearby devices.

The long-term, low-bias stability of large 1T-1AD devices ($V_m \sim$ 1.05V [2-3]) was tested with $V_{WL} \sim$ 3.5V (all applied voltage V_{DUT} appears across the AD). Fig. 4 shows that MIEC ADs maintain low-leakage over hours of exposure, whether in a deep (±230mV) or shallow *un-select* (±350mV) condition (inset). Repeated exposure to the *half-select* (±530mV) condition (Fig. 5, t<70s) has no appreciable effect on any of the leakage conditions, and even prolonged exposure to higher currents (Fig. 5, t>70s) induces only subtle effects on subsequent leakage.

Recovery of low-leakage in MIEC ADs

While Figs. 4, 5 show excellent stability, the SMU is too slow to gauge MIEC AD recovery. With a low V_{WL}, a large first AFG "over-voltage" pulse can force a rapid turn-on (Fig. 6) of a 1T-1AD to a given current level; a second pulse can then probe AD recovery dynamics under read or lower bias conditions (Figs. 7–11).

Fig. 7 shows that after a strong write pulse (50uA for 1us), MIEC AD response is in fact affected. For a read following a write (Fig. 7, top), the MIEC AD simply supplies the usual expected current (∼10uA) instantly, without needing overvoltage acceleration. At much lower bias, however, (Fig. 7, bottom) significantly larger currents than the expected low leakage can persist. Assumably, turn-ON involves shifting Cu (slowly under modest bias, rapidly under overvoltage). Once large currents have been passed, some Cu may remain "latched" in place, altering device response. However, even brief (1us) exposure to 0V restores much of the original low-leakage response (Fig. 8), and negative voltages accelerate this significantly (Fig. 9). Post-write effects are also greatly suppressed if write duration is limited (Fig. 10). Despite this, some sort of explicit post-write recovery sequence is likely to be necessary.

In contrast, recovery after read-level currents is much faster. Fig. 11 shows a 3-pulse sequence, in which two long (4ms) pulses at 600mV surround a brief (1us) pulse at 2V. Since V_{WL} is significantly lower, the maximum current is limited to 6uA per-device (to obtain sufficient SNR here, ten devices along a single column were pulsed in parallel). Before the read pulse and without overvoltage, the current at 600mV slowly builds up to ∼300nA. After the read pulse, leakage has increased by no more than 50%, and exposure to 0V (for even 500ns) completely restores the original leakage characteristics. Fig. 12 quantifies the recovery dynamics after write and read events.

Role of thickness in MIEC AD turn-ON speed

Since these 1T-1AD MIEC ADs are fairly thick ($d_{min} \sim$ 75nm), rapid turn-ON requires significant overvoltage (Fig. 13(a)). Despite the slow native response, turn-ON from *half-select* to 10uA read currents can be sub-50ns (Fig. 13(b)). However, such large overvoltages in the presence of bitline capacitance could lead to read disturbs. "Short loop" devices with proximate BEC contacts allow testing of thinner MIEC ADs [4]. Fig. 14(a) shows that native turn-ON (without overvoltage) speeds up considerably as MIEC ADs get thinner, Even modest pulse-shaping in thin MIEC ADs can readily deliver 100ns read-level (10uA) turn-ON (Fig. 14(b)).

Conclusions

BEOL-friendly Access Devices (AD) based on Cu-containing MIEC materials [1-4] can sustain and move rapidly between *un-selected, half-selected, selected(read)*, and *selected(write)* states. Ultra-low leakage can be maintained over hours, leakage recovery after write (30-50uA) operations requires ∼1us (with read (3-6uA) recovery even faster), read operations can be fast enough for use with MRAM (sub-50ns), and inherently-fast thin MIEC ADs offer similar speeds at modest overvoltages (for minimal read disturb).

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References

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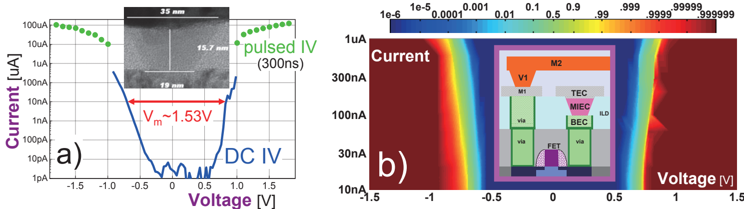

Fig. 1 MIEC-based ADs exhibit the large ON/OFF ratios needed for large crosspoint arrays, showing (a) high voltage margin V_m (for which leakage stays below 10 nA) [3-4], high ON current densities [1,4], ultra-low leakage (< 10 pA) [2-4], good scalability (<30nm CD, <12nm thickness) [4], and (b) tight margins (as well as 100% yield) when integrated on 8" CMOS wafers in large (512kBit) arrays [3].

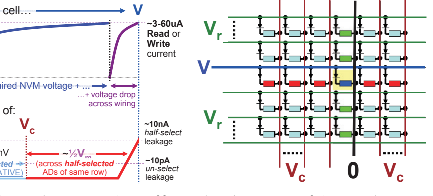

Fig. 2 Voltage on a selected NVM+AD affects 3 other sets of ADs: those in the same row, in the same column (both *half-selected*), and all others (*un-selected*). Each AD must hold ultra-low (~10pA) leakage for hours, maintain modest (~10nA) leakage for seconds, and occasionally pass either read-level (3-6uA) or write-level (30-60uA) currents.

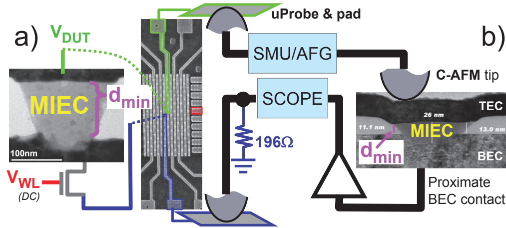

Fig. 3 A Source-Measure Unit (SMU), or an Arbitrary Function Generator (AFG) and oscilloscope, address either small "1T-1AD" MIEC arrays [2-4] or "short-loop" MIEC ADs tested with Conductive-AFM and a nearby BEC contact.

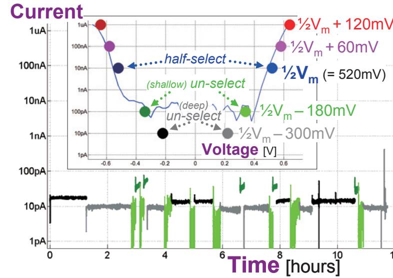

Fig. 4 MIEC ADs maintain low-leakage over hours of exposure, whether in a deep (±230mV) or shallow *un-select* (±350mV) condition.

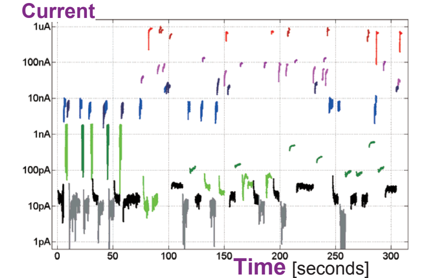

Fig. 5 Repeated 2sec exposures to *half-select* (±530mV) and even higher bias conditions has minimal impact on subsequent leakage.

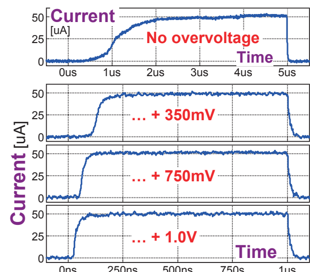

Fig. 6 Turn-ON delay—as induced by RC-delay in establishing a given voltage across a 1T-1AD, followed by the response of the MIEC AD to that voltage—can be greatly reduced by overvoltage.

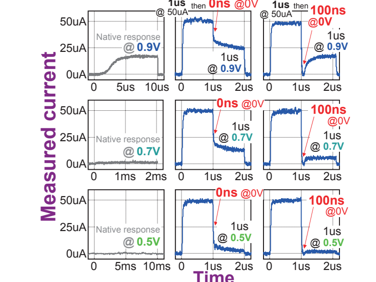

Fig. 7 After a strong write pulse (50uA for 1us), MIEC AD response is affected: devices remain ON, don't require overvoltage acceleration to turn back ON, and at lower voltages where leakage should be undetectable, measurable currents can persist.

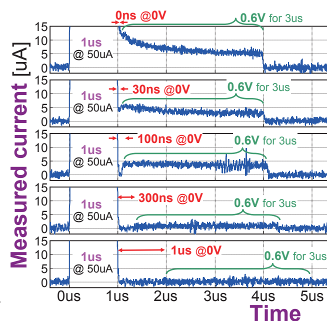

Fig. 8 Even brief (1us) exposure to 0V after a 1us write (50uA) pulse restores much of the original low-leakage response.

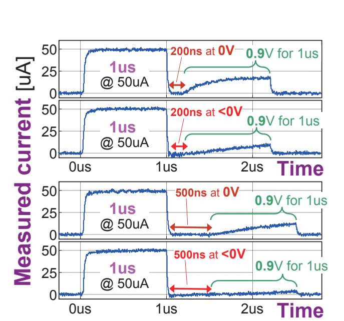

Fig. 9 Exposure to negative voltages accelerates the recovery after a 1us write (50uA) pulse.

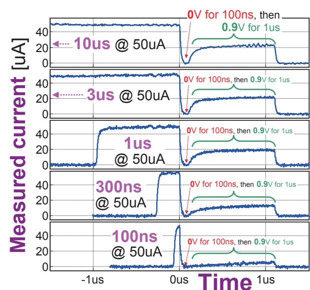

Fig. 10 Post-write effects can also be greatly suppressed by reducing the duration of the 50uA write pulse.

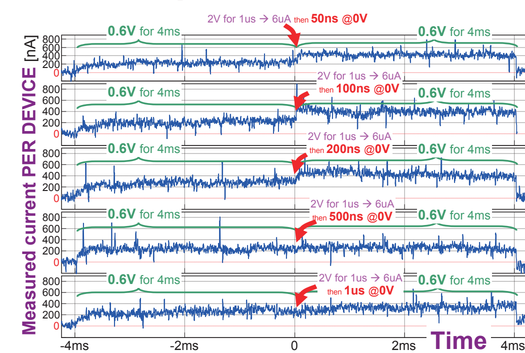

Fig. 11 After a 1us read pulse at 6uA (per-device over 10 ADs), leakage is never more 450nA, or 1.5× the expected static leakage level that would build up over ~1ms anyway.

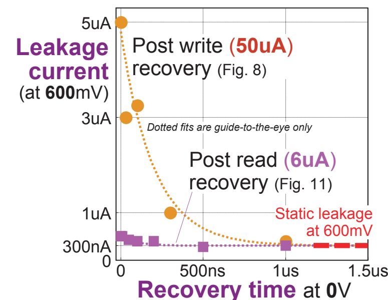

Fig. 12 Restoration of the static IV characteristics (at 600mV) after write (50uA) events takes longer than after a read (6uA).

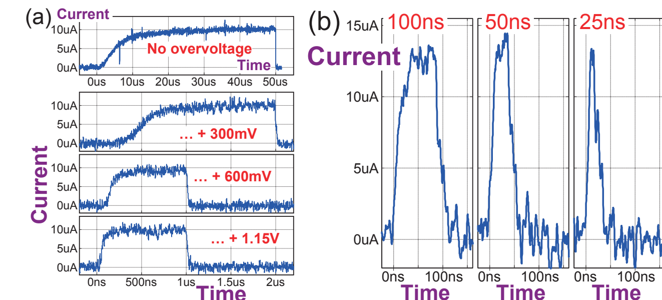

Fig. 13 (a) Despite their slow native response, thick (d_{min} ~75 nm) MIEC 1T-1AD devices can be turned ON rapidly with large overvoltage, allowing (b) the transition from *half-select* to 10uA read currents to occur in <50ns.

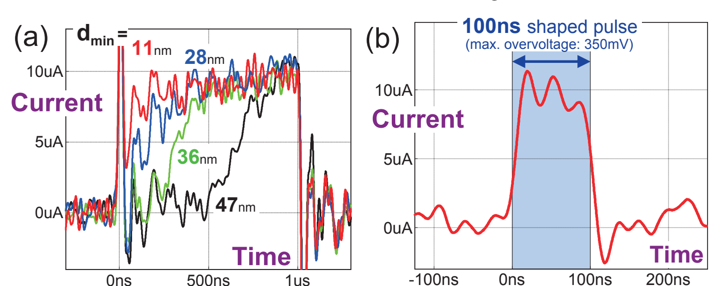

Fig. 14 Thinner MIEC ADs are measurably faster, both in terms of (a) the un-accelerated native turn-ON as well as (b) when accelerated with modest (+350mV) overvoltage.