Phase-change random access memory: A scalable technology

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Nonvolatile RAM using resistance contrast in phase-change materials [or phase-change RAM (PCRAM)] is a promising technology for future storage-class memory. However, such a technology can succeed only if it can scale smaller in size, given the increasingly tiny memory cells that are projected for future technology nodes (i.e., generations). We first discuss the critical aspects that may affect the scaling of PCRAM, including materials properties, power consumption during programming and read operations, thermal cross-talk between memory cells, and failure mechanisms. We then discuss experiments that directly address the scaling properties of the phase-change materials themselves, including studies of phase transitions in both nanoparticles and ultrathin films as a function of particle size and film thickness. This work in materials directly motivated the successful creation of a series of prototype PCRAM devices, which have been fabricated and tested at phase-change material cross-sections with extremely small dimensions as low as 3 nm × 20 nm. These device measurements provide a clear demonstration of the excellent scaling potential offered by this technology, and they are also consistent with the scaling behavior predicted by extensive device simulations. Finally, we discuss issues of device integration and cell design, manufacturability, and reliability.

Introduction

Phase-change materials possess a unique combination of properties that make them promising candidates for the memory material in phase-change RAM (PCRAM) devices. A phase-change material is one that exists in at least two phases with remarkably different properties and can be repeatedly and rapidly cycled between these phases. The amorphous phase is characterized by a low optical reflectivity and high electrical resistivity, while the crystalline phase (or phases) shows high reflectivity and low resistivity. Although the change in reflectivity can be as great as approximately 30%, the change in resistivity can be as large as five orders of magnitude (a 10,000,000% difference).

Even though the principle of applying phase-change materials in a PCRAM cell was demonstrated as long ago as the 1960s [1], the technology has only recently been developed seriously by a number of companies, and first products are about to enter the market. This renewed interest in PCRAM technology was triggered by the discovery of fast crystallizing materials such as $Ge_2Sb_2Te_5$ (GST) or Ag- and In-doped Sb_2Te (AIST) [2, 3]. These materials can crystallize in less than 100 ns, as opposed to the materials used for early PCRAM demonstrations such as $Te_{48}As_{30}Si_{12}Ge_{10}$, which could require 10 μs or more to crystallize [1]. These newer alloys switch faster because the crystallization process generates very little atomic motion [4], compared to the phase segregation that occurs in the earlier Te-rich alloys [5].

In PCRAM, the phase-change material is crystallized by heating it above its crystallization temperature (SET operation), and it is melt-quenched to make the material amorphous (RESET operation). These operations are controlled by electrical current: high-power pulses for the

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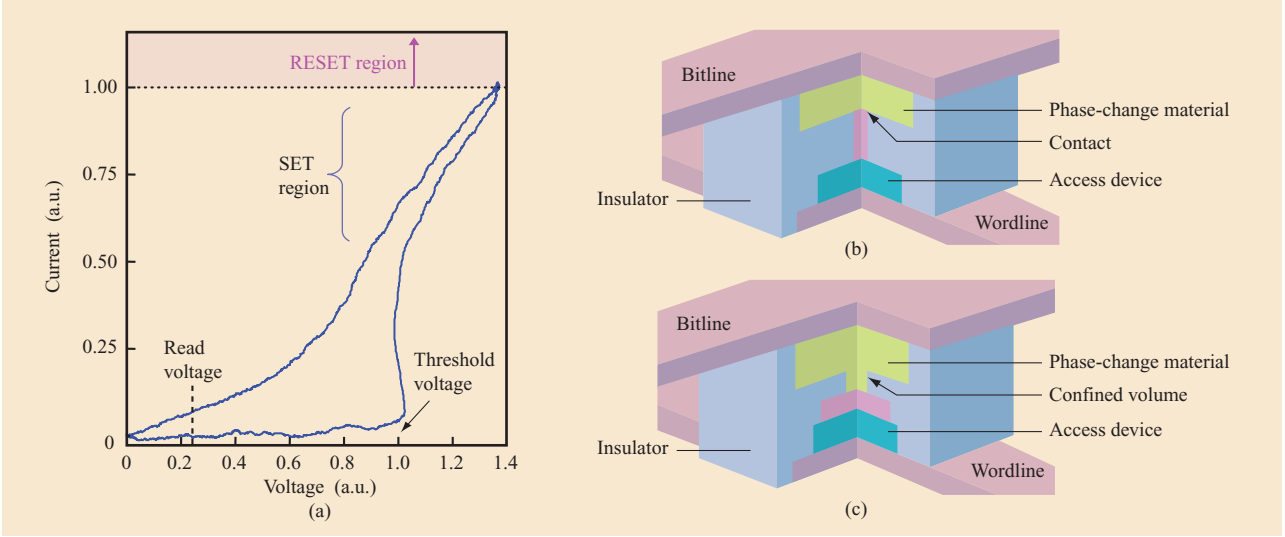

Figure 1

Phase-change device. (a) Typical current–voltage (I–V) curve for a phase-change device, demonstrating the threshold switching and differing amount of electrical power required for SET and RESET operation (a.u.: arbitrary unit). (b) A typical contact-minimized cell, the mushroom cell, forces current to pass through a small aperture formed by the intersection of one electrode and the phase-change material. (c) A typical volume-minimized cell, the pore cell, confines the volume of the phase-change material in order to create a small cross-section within the PCRAM device. (Republished from Reference [6]; ©2006 IEEE.)

RESET operation that places the memory cell into the high-resistance RESET state, moderate power but longer duration pulses for the SET pulse returning the cell to the low-resistance SET state, and finally very low power for retrieving data by sensing the device resistance [**Figure 1(a)**]. Other aspects of Figure 1 are discussed later in this paper.

A critical property of phase-change materials is the threshold switching [7–9]. Without this effect, PCRAM would simply not be a feasible technology, because in the high-resistance state, extremely high voltages would be required to deliver enough power to the cell to heat it above the crystallization temperature. However, when a voltage above a particular threshold V_t is applied to a phase-change material in the amorphous phase, the resulting large electrical fields greatly increase the electrical conductivity. This effect is still not completely understood but is attributed to the interplay between impact ionization and carrier recombination [7]. With the previously resistive material now suddenly highly conducting, a large current flows, which can then heat the material. However, if the current pulse is switched off immediately after the threshold switching, the material returns to the highly resistive amorphous phase after about 30 ns [10], with both the original threshold voltage V_t and RESET resistance recovering slowly over time [10, 11]. If a current sufficient to heat the material above the crystallization temperature but below the melting point is sustained for a sufficiently long time, the cell switches to the crystalline state [Figure 1(a)].

In this paper, we discuss the size-scaling aspects of phase-change memory. PCRAM technology seems to be a promising technology with respect to such scaling.

Scaling of phase-change memory

The history of the solid-state memory industry and the semiconductor industry as a whole can be thought of as an incessant march along Moore's Law to smaller device dimensions enabling ever-increasing system functionality. In the case of memory, increased system functionality is manifested in the form of more megabytes (and now more gigabytes) in the same package size. Throughout this extensive history, extrapolation from the recent past has proven to be amazingly reliable for predicting near-future developments. Thus, the memory products that will be built in the next several years have long been forecast [12].

Beyond the near future, however, while the *size* of what should be possible to fabricate can be estimated, for the first time in many years it is not clear exactly *what* should be built, particularly in the area of nonvolatile memory (NVM), currently dominated by flash memory technology. Thus, the industry faces the prospect of a costly and risky switch from a known and established technology to something much less well known. Understandably, industry will often attempt to avoid such leaps, when possible.

The problem is not a possible failure to create a successful first product, because such failures are usually discovered at the advanced research or early development stage, when the level of investment is small and multiple alternative approaches are still being pursued. Instead, the disastrous scaling scenario is one in which the new technology works perfectly well for the first generation yet is doomed to failure immediately afterward. If only one or two device generations succeed, the NVM industry, having just invested heavily in this new technology, will be forced to make yet another switch and start the learning process all over again.

Thus, scaling studies are designed to consider the far future of the device road map, to try to uncover the roadblocks that may hinder a potential NVM technology at sizes much smaller than what can be built today. In the context of phase-change memory, we must consider the purpose the PCRAM cell will serve, along with possible failures, as the size of the cell scales down.

Critical device characteristics for a PCRAM cell include widely separated SET and RESET resistance distributions (necessary to create a margin of separation in order to avoid noise on fast readout), the ability to switch between these two states with electrical pulses that can be produced with the access device, the ability to read, or sense, the resistance states without perturbing them, high endurance (allowing many switching cycles between SET and RESET), long data retention (usually specified as a 10-year data lifetime at some elevated temperature), and fast SET speed (the time required to recrystallize the cell from the RESET state). Data retention usually depends on the ability of a cell to retain the amorphous RESET state by avoiding unintended recrystallization. An additional aspect that can be of significant importance is the ability to store more than one bit of data per cell, because this allows technologists to increase effective density without decreasing the feature size.

PCRAM cells have many possible points of failure. First, the underlying physics of the phase-change process could be completely different when the entire memory device essentially consists of interfaces only. Second, the threshold voltages for ultrascaled devices might be too close to the read voltages, thus creating a risk of accidental overwrites. If one looks sufficiently far into the future, the number of total atoms in a memory cell will become countable, which will likely require major rethinking with respect to doping with defect atoms, crystallization, melting and heat flow, and electrical tunneling effects.

In the next few technology generations, the most serious consideration is probably the need to ensure that the large currents required to switch PCRAM cells can be supplied by the associated access device. In a full memory array, an access device such as a diode or transistor must be included at each memory cell to ensure that the read and write currents on each bitline interact with only one memory device at a time. The amount of current that this access device can supply essentially sets the requirement for the phase-change memory element RESET current. One way to relax this requirement is to simply make the access device larger so that it can drive a larger current. However, because this choice sacrifices memory density and subsequently increases the cost per megabyte, this solution is not economically viable for a prospective memory technology.

A more tenable choice involves the use of the largest access device that does not sacrifice any density, along with a design of the phase-change memory cell such that the only current path through the device passes through a very small aperture. As this aperture shrinks in size, the volume of phase-change material that must be melted (and quenched into the amorphous state) to completely block the aperture is reduced. In turn, this decreases the power (and thus, the current) requirements. If this current is sufficiently low, then a minimum-size access device can provide sufficient power to switch the cell from its SET state to its RESET state. Although returning to the SET state involves exceeding the threshold voltage, the amount of power (and current) in the SET pulse is typically 40–80% of the RESET pulse. Thus, the RESET pulse usually must be considered when determining whether the access device will supply sufficient current, while the SET pulse is typically the factor that dictates the write speed of PCRAM technology.

Two general categories of cell structures exist for implementing a sublithographic aperture. One category involves the control of this cross-section by the size of one of the electrical contacts to the phase-change material [contact minimized, **Figure 1(b)**] [13–19]. The other category involves minimizing the size of the phase-change material itself at some point within the cell [volume minimized, or confined, **Figure 1(c)**] [6, 13, 20–26]. When compared to contact-minimized cell structures, volume-minimized phase-change material structures have the advantage of offering a potentially lower RESET current for a given critical dimension [13, 21, 24], as well as the possibility for enhanced endurance. This possibility is supported by the observation that many failure and degradation mechanisms for PCRAM cells are associated with the interface between the phase-change material and one of the surrounding materials [27]. It is beneficial to keep the switching volume as contained as possible within the phase-change material and thus away from the electrodes.

On the other hand, in addition to some processing advantages mentioned in the section "Device integration issues of scaling," advantages exist for the contact-

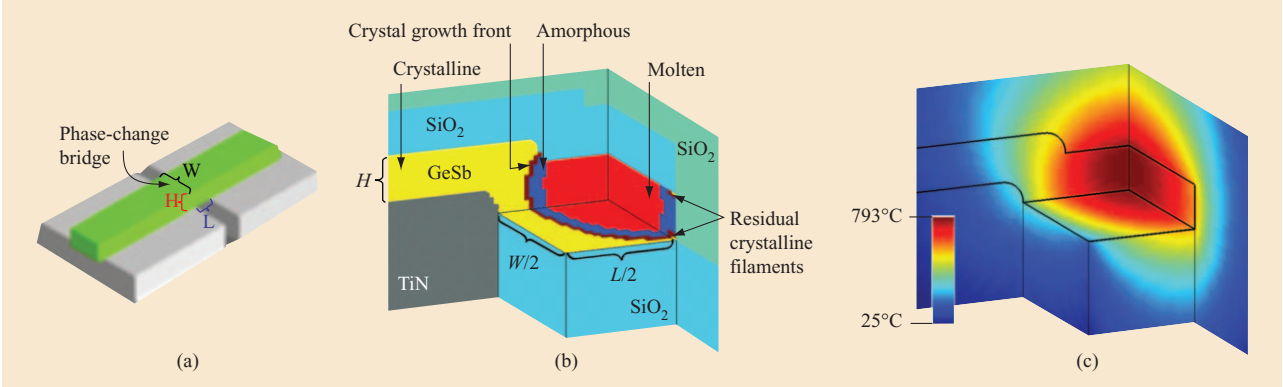

Figure 2

In the phase-change bridge (PCB) memory cell, (a) the cross-sectional area ($W \times H$) has only one dimension that depends on lithographic patterning, making it possible to greatly reduce the second dimension via ultrathin films. (b) Simulated 3D distribution of material phase. (c) Temperature distribution within a PCB memory device during a RESET pulse, showing the receding melting spot as the device just begins to cool. A slightly higher pulse current would have melted the residual crystalline filaments at the device periphery, leading to a successful RESET. (Republished from Reference [6]; ©2006 IEEE.)

minimized design. For instance, because the switching volume occurs where a large expanse of phase-change material meets a narrow electrode, heat loss is reduced in both directions. In one direction, heat loss is low because of the inherently low thermal conductivity of the phase-change material. In the other direction, heat loss is low because the small cross-section of the electrode helps keep the overall thermal resistance high despite its high thermal conductivity.

Because of the large number of factors that can influence the RESET current, predictive numerical simulations are important. A number of studies have used analytical equations [28–31], finite-element techniques [21, 32–34], and finite-difference techniques [6, 35] to analyze either PCRAM cells or the phase-change material. Pirovano et al. [13] studied the RESET current and the thermal proximity effect of scaled PCRAM using both simulation and experiment. Although analytical techniques are attractively simple and work well for explaining the incubation of new crystalline nuclei [28] or threshold switching [29], it is difficult to include the effects of inhomogeneous temperature distributions and temperature-dependent resistivity, which critically affect the RESET current through their effect on the dynamic resistance of the cell. Finite-element techniques can include these effects but are difficult to extend to three-dimensional cell designs. Finally, even though nucleation is unlikely to have an effect during the fast RESET pulse, recrystallization at the end of a RESET pulse does play an important role in the value of the RESET current, especially for the fastest-crystallizing phase-change materials that are potentially of the most use for applications. The best-case scenario involves a simulation tool that provides results that could potentially be compared to fast electrical SET and RESET experiments, slow thin-film crystallization experiments, and optical-pulse experiments performed with the same material.

From our experience with such a simulation tool [6], the RESET condition is not dictated by the maximum temperature at the cell center, but by what happens at the edge of the cell. For instance, as shown in **Figure 2**, a voltage pulse just below the RESET condition invariably results in some small portion of the limiting cross-sectional aperture remaining in the crystalline state, usually at the extreme edges of the cell [6]. (The cell concept shown here, called the *phase-change bridge* [Figure 2(a)], is described in detail in the section "Scaling demonstrator: The phase-change bridge.")

In general, aside from the obvious choice of reducing the phase-change critical dimension, the best way to reduce the RESET current is to improve the efficiency with which injected electrical power heats the cell. Another popular way to decrease the RESET current is to increase the overall resistance of the cell by increasing the series resistance of the contact electrode [36].

Other considerations that need to be taken into account for scaling include possible decreases in supply voltage, concerns about whether devices will be able to retain data throughout the desired 10-year lifetime (at a maximum temperature that depends on the particular application), and sudden increases in failure mechanisms that could possibly arise at some future technology node (i.e., technology generation). While failure mechanisms are difficult to predict, Pirovano et al. [13] showed that at

least out to the 65-nm node, the thermal cross-talk between cells should remain sufficiently low that a 10-year lifetime will not be significantly reduced by writing data to neighboring cells.

Phase-change materials

One of the most critical aspects of PCRAM technology involves the memory material itself. Most phase-change materials are chalcogenides, containing at least one element from group 6 of the periodic table, with GST being the most commonly used and most widely studied material. A notable exception is GeSb, which though not a chalcogenide is still a very promising phase-change material. Dozens of different phase-change materials have been developed [37–39], and the choice of available materials can be further widened by doping these materials [23, 40–42]. Examples of phase-change materials being investigated for PCRAM include the following: Ge-Te [43], $GeSeTe_2$ [44], $AgSbSe_2$ [45], Sb-Se [46], Ag-In-Sb-Te [47], and other Sb-Te variants [23, 48], along with a wide variety of dopants.

Researchers involved with phase-change technologies started to build devices using GST because it was one of the most commonly applied materials in optical storage; however, these materials had been originally selected by developers of optical storage because of the advantageous optical properties of the materials. Not surprisingly, these same materials have some disadvantages within PCRAM applications. For example, this large optical contrast (desirable for optical storage) is directly correlated with a large difference in mass density between the amorphous and crystalline phases [49], which can be as high as 7% or 8% for GST [50]. Such a large mass density change on switching could in fact be detrimental in a solid-state device, while optical contrast is of no consequence.

For successful development of PCRAM technology, the phase-change material needs to fulfill a number of properties simultaneously. Phase-change materials for PCRAM must have the appropriate crystallization speed. They should crystallize fast (e.g., in a few tens of nanoseconds) but not too fast; otherwise, melt-quenching becomes impossible. They should have relatively high resistivity in the crystalline phase in order to reduce the RESET current, yet the difference between the resistivities of the two phases should still be very large (greater than a factor of 100) in order to maintain a high on/off ratio. While a relatively low melting point is desirable for a reduction of the RESET current, a phase-change material needs to retain data at the operation temperature of the memory (~80–90°C for embedded memory and as high as 150°C for automotive applications). Thus, the crystallization temperature of a suitable material must be substantially higher than the operating temperature. High cyclability is of great importance for many applications, so the material should not chemically react with its surroundings or deteriorate during repeated cycling. Finally, it should be possible to deposit the optimum material using CMOS-compatible deposition techniques such as sputter deposition or chemical vapor deposition.

Scaling properties of phase-change materials

One aspect of scaling to consider for PCRAM technology is the behavior of the materials themselves when dimensions decrease. It is known that thin films or nanoparticles of a given material can have very different properties from their bulk counterparts. In order to predict the potential behavior of highly scaled PCRAM, it is important to find out how and at what film thickness or nanoparticle size the properties of phase-change materials might be influenced by size. Important properties that can be influenced by size are the crystallization temperature and the melting point, and this scaling behavior is likely to be a function of material as well.

Scaling of the materials has been studied by shrinking dimension (thin films) [51–54], two dimensions (nanowires) [55–59], and three dimensions (nanoparticles) [60–67] for a variety of phase-change materials. Thin films of GST and GeSb were studied with time-resolved x-ray diffraction (XRD). The films were deposited at room temperature and were amorphous as deposited. We found that the crystallization temperature increases as film thickness is reduced [51]. Films that are thinner than about 20 nm showed a higher temperature at which crystallization occurs than thick films and bulk material. For the thinnest films that still showed clear XRD peaks (1.3 nm thick for GeSb), crystallization occurs at about 300°C, while thick films crystallize at about 235°C. This increase in crystallization temperature indicates that data loss due to nucleation of new crystal nuclei within the amorphous portion of a scaled-down cell in the RESET state should actually be less likely than in a larger cell.

For thin GST films, the amorphous-fcc (face-centered-cubic) phase transition also shifts to higher temperatures for films thinner than 20 nm, and for films thinner than 3.6 nm, the fcc phase is no longer formed. Interestingly, the hexagonal phase is still formed in these very thin films of 3.6 nm and 2 nm, but no crystallization was observed in films thinner than 2 nm. As we discuss in the next section, it is indeed possible to fabricate functioning PCRAM cells with films as thin as 3 nm. Recording of information has also been demonstrated using 18-nm thin GST films [53], with recording densities up to 3.3 Tb/in^2 by applying a nanoheater atomic force microscopy (AFM) tip. With ultrathin GST films (1–5 nm), the smallest crystalline recording marks in an amorphous film that could be produced by an AFM tip were found to be about 10 nm in diameter [54], although these smallest

marks disappeared within minutes. On the other hand, slightly larger marks (20 nm) were stable for at least one hour. The reverse process was also demonstrated, and amorphous marks as small as about 10 nm were also recorded using AFM and scanning tunneling microscopy (STM) [52].

GST [55], GeTe [56–58], In_2Se_3 [59], and Sb_2Te [58] phase-change nanowires have been grown by the metal catalyst-mediated vapor-liquid-solid method. These nanowires were single crystals, with diameters ranging from 20 to 200 nm, depending on the size of the Au catalyst nanoparticles. In one case [58], GeTe nanowires with a helical structure were formed. Sun et al. [57] also found that the melting point of GeTe nanowires was significantly reduced to 390°C, which may be compared to the bulk melting point of GeTe of 725°C. Researchers have observed a reduction of the melting point for In_2Se_3 nanowires [59], which melted at 680°C compared to a melting point of 890°C for bulk In_2Se_3. Switching devices were fabricated [55, 56] by contacting the GeTe nanowires employing a focused ion beam (FIB) technique to deposit Pt electrodes with a 2-μm separation on a nanowire. In other words, two Pt contact pads are formed by the FIB, and these contacts can be used to make a connection with the larger metal tips of a tester in order to test the device. These devices showed clear threshold-switching characteristics typical for phase-change devices and could repeatedly be switched between the amorphous and the crystalline phase using an electrical current pulse.

Phase-change nanoparticles have been fabricated and studied using a variety of methods. Pulsed-laser ablation was used to fabricate GST nanoparticles with sizes between 5 and 50 nm [57, 62, 63]. PCRAM devices have been fabricated using multiple layers of GST nanoparticles produced by laser ablation [57], and threshold switching as well as repeated switching of the devices has been demonstrated. Yoon et al. [63] reported that for particles exposed to 100°C, 200°C, 300°C, and 400°C, in all cases the particles had crystalline parts in the fcc phase, but they also observed other crystalline phases, presumably due to off-stoichiometric Ge-Sb-Te regions. Choi et al. [62] observed that crystallization of the nanoparticles occurred for temperatures between 200°C and 300°C, and that nanoparticles crystallized at these temperatures showed both the fcc and the hexagonal phase, while nanoparticles heated to temperatures higher than 400°C showed only the fcc phase. This is surprising because it has been shown that the fcc phase is the metastable phase in thick films and bulk GST, appearing at about 150°C and transformed into the stable hexagonal phase at about 350–400°C [68].

The crystallization behavior of large arrays of phase-change nanoparticles of various materials (GST, N-doped GST, GeSb, Sb_2Te, and AIST) fabricated by electron-beam lithography have been studied using time-resolved XRD [67]. In this study, researchers observed that all nanoparticle arrays with particle sizes between 20 and 80 nm exhibited clear crystallization at temperatures similar to thick films of the same material with the exception of Sb_2Te, which showed an increased crystallization temperature (40°C higher) compared to thick films. In particular, GST phase-change nanoparticles exhibited only the fcc phase for the smallest particles (20 nm), while larger particles exhibited a behavior similar to thick films and bulk material [67]. As mentioned earlier, GST thin films seem to behave differently from GST nanoparticles, with the thinnest films forming only the hexagonal phase but not the fcc phase.

To further reduce particle size, self-assembly-based lithographic techniques have been applied to fabricate phase-change nanoparticles [64–66]. Self-assembled PS-b-P4VP (polystyrene-b-polyvinylpyridine) on top of an amorphous GeSb phase-change film was used to locally grow SiO_2 dots on top of the P4VP domains [64, 65]. Reactive ion etching and ion milling were then applied to transfer the pattern into the GeSb using the SiO_2 dots as a hard mask, which can resist the subsequent etching and milling processes. Time-resolved XRD performed on the nanoparticle arrays demonstrated that these 15-nm-diameter particles clearly crystallize at a temperature that is 15°C lower than comparable thin film. **Figure 3** shows the intensity of diffracted x-ray peaks acquired at an x-ray wavelength of 1.797 Å as a function of temperature during a 1°C/s heating of a GeSb phase-change nanoparticle array fabricated through self-assembly, and a cross-sectional bright-field transmission electron microscopic (TEM) image of the same GeSb nanoparticles. In another experiment, PS-b-PMMA [polystyrene-b-poly(methylmethacrylate)] films have been used, with phase-change nanoparticles fabricated by PMMA removal, deposition into the PS-b-PMMA template, and lift-off (i.e., removing the polymer) [66]. AIST nanoparticles of about 20 nm in diameter have been obtained that showed a crystallization temperature of 175°C, slightly higher than a blanket film (165°C).

A very different and nontraditional way of depositing phase-change materials involves the spin-on method. Novel spin-on phase-change materials have been developed [69, 70], and their excellent via-filling capabilities have been demonstrated [70]. By combining spin-on materials and self-assembly (GeSbSe spun-on phase-change material on a PS-b-PMMA template, with PMMA removal and subsequent lift-off), phase-change nanoparticles were produced that showed a crystallization temperature 35°C lower than for thick spin-on films.

Some of the smallest phase-change nanoparticles (sub-10-nm nanoparticles) that have been reported have been synthesized by solution-based chemistry [71]. These GeSe particles were crystalline after synthesis and monodisperse compared to particles fabricated by laser ablation. More studies are required to evaluate the properties of these particles and their potential to serve as memory material, but the fact that these small particles can be crystalline and show narrow size distributions makes them interesting candidates for future PCRAM applications.

Scaling demonstrator: The phase-change bridge

There are several goals for studying the scaling behavior of a PCRAM device. Although simulations and analyses have long predicted that the RESET current should be reduced when the device dimensions are reduced [16], the exact value and rate of this reduction depends significantly on simulation parameters that are not always well known. Thus, the fabrication of devices that vary in size is critical for the quantitative calibration and verification of such models. In addition, experimental demonstration of prototype devices provides tangible proof that very small phase-change memory devices do indeed work. A number of aspects not easily apparent in simulation can be evaluated, such as changes either in the degradation mechanisms or in the phase-change dynamics in the presence of increased surface and interface effects.

Several groups have studied phase-change memory scaling [13, 23]. By measuring the RESET current experimentally, Pirovano et al. [13] showed that even when the contact area between the phase-change materials and the electrode is only about 300 nm^2, devices still function properly. Lankhorst et al. [23] described a phase-change line device with cross-sectional areas as small as 225 nm^2 that could be switched repeatedly [23]. However, if we assume that the sublithographic size of the phase-change critical dimension will be equal to 30% of the smallest achievable lithographic dimension [12], then these 15-nm phase-change critical dimensions roughly correspond to a 45-nm lithography node, which will likely be in use by the flash memory industry as soon as 2009 [12]. In order to determine how PCRAM might operate further into the future, it is of great interest to try to further decrease device cross-section.

The device we have implemented in order to study scaling in actual devices, called the *phase-change bridge* (PCB) and shown in Figure 2(a), consists of a narrow line of ultrathin phase-change material bridging two underlying electrodes [6]. Unlike in earlier line-device concepts [23], the electrodes are formed very close together in order to obtain a reasonable threshold voltage and are separated by a small oxide gap that defines the bridge length L. The cross-sectional area ($W \times H$) depends linearly on lithographic patterning, offering both reduced sensitivity to variations in the critical lithographic dimension and an alternative path for scaling to future technology nodes via ultrathin films.

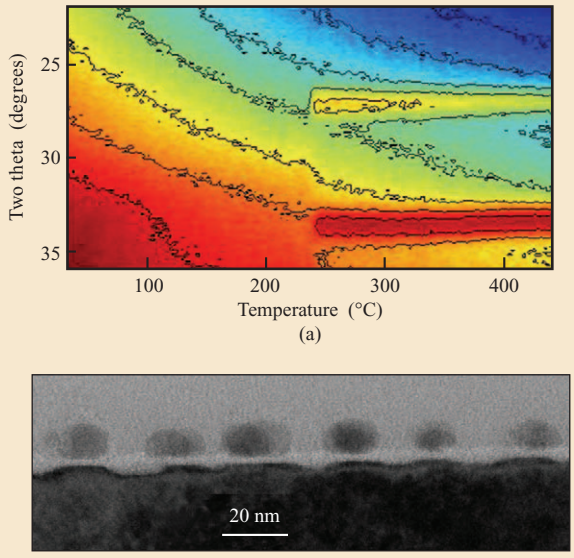

Figure 3

GeSb nanoparticles. (a) Intensity of diffracted x-ray peaks as a function of temperature during a 1ºC/s heating of GeSb phase-change nanoparticle arrays fabricated using self-assembly-based lithography. The data were acquired at an x-ray wavelength of 1.797 Å. (b) Cross-sectional bright-field TEM image of the same GeSb nanoparticles, demonstrating that sub-20-nm-sized particles crystallize at temperatures that are similar to bulk material.

The process flow for the device in our study is shown in **Figure 4**, together with representative scanning electron microscope and TEM images. First, conventional 248-nm KrF lithography and etching was used to fabricate two parallel trenches in SiO_2 separated by a very narrow SiO_2 layer (from 40 nm to 500 nm). After filling in the trenches with thick Ti/TiN by sputter deposition and subsequent chemical-mechanical polishing, wafers were obtained with two TiN electrodes separated by a small SiO_2 gap [Figure 4(a)]. Doped GeSb phase-change material with thicknesses between 3 and 10 nm was then deposited using magnetron sputtering, followed immediately by a 10-nm SiO_2 cap layer to prevent oxidation of the phase-change material [Figure 4(b)]. Electron-beam lithography was then used to define the bridge structures with widths between 20 and 200 nm. After the final ion milling step, another cap layer of 5 nm of Al_2O_3 was deposited onto the device without breaking vacuum to prevent oxidation

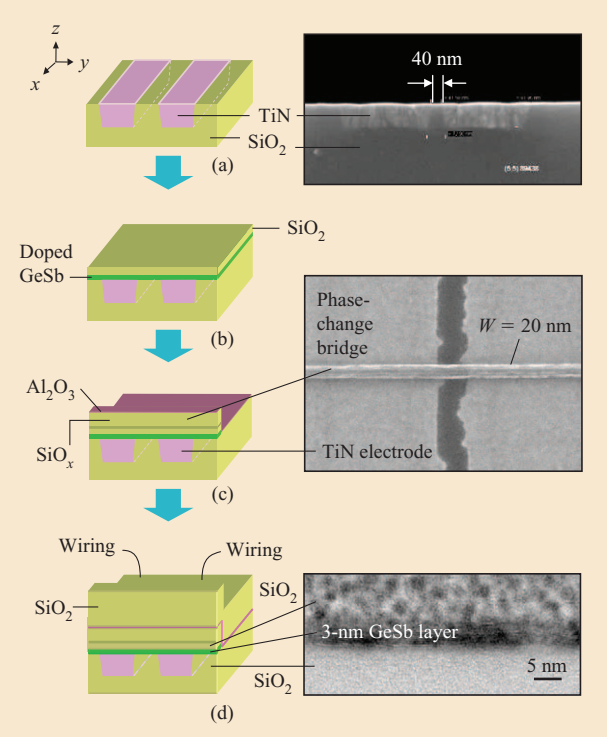

Figure 4

Schematic 3D plots are illustrated after each step for fabricating the bridge device. (a) 3D plot and cross-sectional SEM (scanning electron microscope) image after TiN electrode fabrication. (b) 3D plot after SiO_2 deposition. (c) 3D plot and a top-view SEM image after Al_2O_3 encapsulation. (d) Schematic plot and cross-sectional TEM image after full fabrication. (Republished from Reference [6]; ©2006 IEEE.)

[Figure 4(c)]. To protect the whole device, a thick capping layer (50 nm of SiO_2) was deposited before the device was wired for testing [Figure 4(d)].

These PCB devices were electrically tested using a custom apparatus designed for prototype PCRAM devices. An arbitrary-waveform generator was used to produce current pulses with rise and fall times shorter than 2.5 ns. Such pulses are required because the doped GeSb material shows very fast recrystallization, as fast as 10–20 ns in optical characterization experiments [6]. The current–voltage characteristics of these devices exhibit both threshold switching and proper device performance (switching between SET and RESET states), even at the smallest cross-sectional areas of 60 nm^2 ($H = 3$ nm, $W =$ 20 nm). This rectangular cross-sectional area corresponds to a cylindrical phase-change critical dimension of 9 nm, commensurate with a minimum lithographic feature size of 30 nm. Thus, these PCB devices provide strong experimental evidence that PCRAM devices could potentially scale at least through the 32-nm device generation, which the flash memory industry is expected to reach in the year 2013 [12].

SET pulses as short as 40 ns could be used to switch the PCB without sacrificing the ratio between the RESET and SET state resistances. Because such speeds are not easily obtained even in large GST-based devices, these results are due to the inherently fast switching found in doped GeSb phase-change materials. Optical testing of the raw material [6] also shows significant speed improvements compared to the GST material. Thus, this doped GeSb material offers a unique combination of fast switching, a very high difference in resistivity between the amorphous and crystalline phases (more than four orders of magnitude), high crystallization temperatures, and even the capability of operating using phase-change material thicknesses as small as 3 nm.

As predicted by simulations, the RESET current scales directly with the cross-sectional area of the device. A comparison of experimental results with simulation results for RESET current is shown in **Figure 5**. For the smallest devices fabricated in this study, with a cross-sectional area of 20 nm by 3 nm, the RESET current was as low as approximately 80 μA. As predicted, the lowest RESET current was not obtained with the shortest device lengths [6]. This effect arises from a balance between the excessive heat loss to the metal electrodes that occurs at short lengths and the poor power efficiency that comes from distributed heating of a long PCB.

With careful design of the surrounding material and structure, the RESET current can potentially be further reduced. For instance, by modifying the process described above, we were able to fabricate PCB devices with 5-nm-thick TaN electrodes (instead of 80-nm TiN). This allowed us to reduce the RESET current by roughly 40% (Figure 5).

Typically, PCB devices could be cycled through more than 10,000 SET–RESET cycles. Thermal retention was tested by measuring the resistance of a PCB device programmed into the RESET state while heating the device. As expected from the measured dependence of resistivity on temperature in doped GeSb, the device resistance decreases while heating. After heating to 175°C at a rate of 1°C/s, the device was cooled and the resistance was found to have returned to a high-resistivity state. A device fabricated from GST would have fully crystallized at these temperatures, losing the stored data. However, the final resistance in the doped GeSb device is approximately only 50% of the value of the initial resistance; thus, some small amount of recrystallization has taken place. Doped GeSb has an advantage because it moves the point at which data loss occurs to higher temperatures.

Device integration issues of scaling

Prototype devices such as the PCB are ideal vehicles for fast testing of new materials because the fabrication turnaround time can be very short. This is especially true in comparison to the integration of arrays of PCRAM cells, each fabricated with its own access device in a full CMOS process. For such fully integrated wafers, a number of other concerns must be addressed. As mentioned earlier, the need to minimize the RESET current required by the phase-change memory cell and to maximize the current supplied by the access device are key issues for achieving a small size for the phase-change memory cell. In addition, while the read voltage, the RESET pulse, and the SET pulse can be optimized for the average memory cell, variations between cells and between access devices must be minimized so that these same choices can be used to successfully operate all the cells in the memory array.

Although alternative schemes exist [72], a diode or transistor is typically used as the access device. While a diode can provide a current-to-cell size advantage over a planar transistor at sizes as low as those used at the 16-nm node [73], the diode scheme is more vulnerable to errors induced by writing data to adjacent cells because of bipolar turn-on of the nearest-neighbor cells [25]. A 5.8-F^2 PCRAM diode cell has been demonstrated using a 90-nm technology in which the diode was able to supply 1.8 mA at 1.8 V [25]. (The term F refers to the smallest lithographic feature size of the respective lithographic technology node.) In comparison, a 90-nm 10-F^2 tri-gate FET could only supply approximately half of this current [25].

In order to fabricate a phase-change memory cell that will work even with these small currents, an innovative integration scheme is needed that creates a highly sublithographic, yet controllable, feature size. Subtle variations in cell design may have a significant impact on critical device characteristics, including endurance, retention, SET and RESET resistance distributions, and SET speed. The cell design must be scalable as well as highly manufacturable, because scaling implies not only a decrease in the physical dimension of the memory cell, but also an increase in the number of memory cells per chip. Finally, in order to maximize the number of bits per cell, a cell structure that allows multibit functionality is highly desirable [24, 74].

Many different types of cell structures have been proposed with the aim of not only minimizing the RESET current, but also improving reliability and performance and reducing the variability. Most notable are the mushroom cell [16], the pillar cell [24], the bridge cell [6], the microtrench cell [14], the pore cell [20, 22, 26], and the ring bottom electrode mushroom cell [15, 17–19].

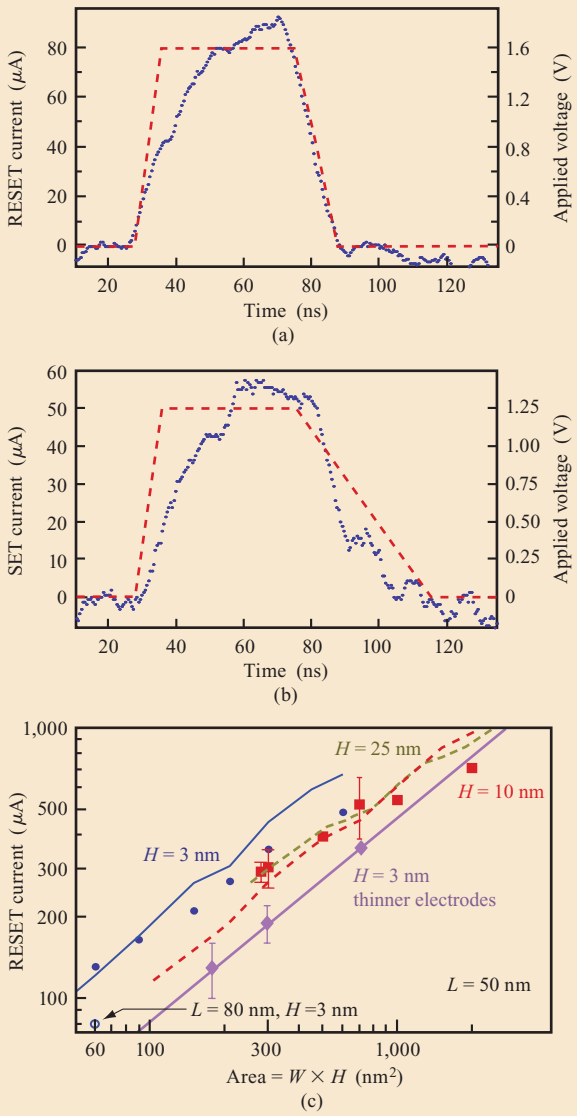

Figure 5

Typical measured current traces for (a) RESET and (b) SET steps of a prototype phase-change bridge memory cell with a 60-nm^2 cross-sectional area (H = 3 nm, W = 20 nm, L = 50 nm) and minimal encapsulation, corresponding to RESET (or SET) resistances of 500 kΩ (or 95 kΩ). The red dashed line indicates applied voltage, as labeled on the right y-axis. The blue dotted line indicates the device current, as labeled on the left y-axis. (c) Measured (symbols) and simulated (lines) RESET current of prototype phase-change bridge memory cells as a function of bridge width W, for L = 50 nm and H = 3, 10, and 25 nm (simulation only). For comparison, the open symbol shows our lowest achieved RESET current (with 80-nm thick TiN electrodes) of roughly 80 μA. The purple diamonds, along with a fit through the data to guide the eye, show the reduction in RESET current made possible when reducing the heat loss through the electrodes by reducing electrode thickness and changing from TiN to TaN. (Republished from Reference [6]; ©2006 IEEE.)

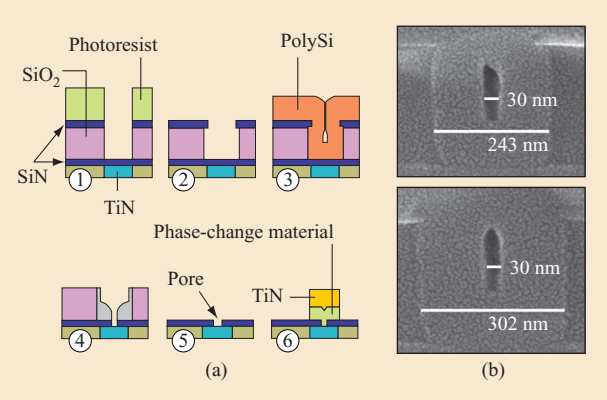

Figure 6

Sublithographic features. (a) A sublithographic-size lithography-independent feature is fabricated using the keyhole-transfer process in a sequence of steps described in the text. (b) SEM cross-sectional image corresponding to step 3, showing keyholes for two different sized lithographically defined holes. Because the keyhole size does not depend on lithography, the phase-change critical dimension is decoupled from any lithographic variability.

When compared to contact-minimized cell structures, volume-minimized phase-change material structures have some potential advantages in terms of RESET current for a given critical dimension and in endurance (because the switching volume is kept away from material interfaces). However, the fabrication of such volume-minimized structures offers significant challenges, either in the filling in a sublithographic-sized feature with the phase-change material (microtrench and pore cells) or in the etching of a sublithographic line (bridge cell) or pillar (pillar cell) of phase-change material. Standard PVD (physical vapor deposition) sputter deposition techniques have been successful at filling low aspect-ratio pores [20, 26], and a deposition/etch/deposition process has been demonstrated for filling a 50-nm bottom critical-dimension 2:1 aspect-ratio pore [22]. A recent advancement in the confined phase-change memory cell was a demonstration of a high aspect-ratio pore cell filled with chemical vapor deposition (CVD) GST, polished after GST deposition, and capped with a top electrode material [75]. This fill-and-polish scheme has the additional advantage of avoiding possible damage of the phase-change material caused by the reactive ion etching process [25] that is normally required to isolate the device from its neighbors along adjacent bitlines.

The main advantage of the contact-minimized cell structures is the relative ease of fabrication associated with the phase-change material deposition and isolation processes. A sublithographic bottom electrode integration scheme (such as that used for a mushroom cell) forms a flat surface on which the phase-change material can be deposited with a standard PVD sputter deposition. In addition, the flat surface eliminates possible sources of stress associated with topography that could degrade reliability. Contact-minimized structures also naturally allow an optimization of the encapsulation material surrounding the phase-change material, since the encapsulating material can be deposited directly after the phase-change material isolation, independent of the previous processes. This encapsulation is important, as it has been found to help avoid oxygen penetration that can oxidize the interface between the bottom electrode and the phase-change material [18].

Various methods have been introduced to create sublithographic features. The creation of a pillar cell begins with a lithographically defined pillar of photoresist that is reduced in size through the use of a trimming reactive ion etching [24]. The mushroom cell and the microtrench cell make use of a lithographically defined hole [15] or trench [14], and the size is reduced using a spacer process. However, these methods tend to produce a sublithographic feature that inherits the critical-dimension variation associated with the lithographic dimension. Because the microtrench cell includes a bottom electrode whose line width is determined by deposition rather than lithography, only one of the two critical dimensions of the microtrench cell is dependent on lithography (as is the case for the PCB). The ring bottom electrode mushroom cell was introduced to reduce the dependence of the effective contact area of the bottom electrode on the variability of the size of the lithography- and spacer-defined contact hole [15], because the contact area of a thin annulus varies only linearly with its diameter. However, in all of these approaches, lithographic variations directly result in variations in diameter, which in turn cause the cell resistance to vary from device to device. Such variations have two effects. First, resistance variations reduce the distinction between the SET and RESET states, potentially leading to bit errors on readout. Second, variations in resistance will tend to change the temperature produced by a particular applied voltage, which increases the worst-case RESET pulse amplitude, reduces endurance by exposing some cells to much more RESET power than they really require, and unnecessarily complicates the design of a SET pulse that can successfully switch any cell in the memory array.

We have developed a keyhole-transfer process [26] that fully de-couples the variation associated with lithography from the sublithographic feature size. **Figure 6(a)** shows how the keyhole-transfer process creates a sublithographic critical dimension that is essentially independent of the original feature size by

combining accurate etch-back with conformal deposition into a lithographically defined hole. In step 1, a lithographically defined hole is etched into a SiN-SiO_2-SiN stack stopping on the bottom SiN. Then, a selective wet etch (step 2) is used to recess the SiO_2 layer. In step 3, a highly conformal polySi film is deposited, producing a sublithographic keyhole in the polySi, whose diameter is equal to the recess of the SiO_2 layer. This keyhole is transferred (step 4) into the underlying SiN layer to define a pore. The SiO_2 layer and polySi are removed with a wet etch (step 5). The phase-change and top electrode (TiN) materials are deposited, and finally the cell is patterned (step 6) for isolation. **Figure 6(b)** demonstrates the ability to create a keyhole with a sublithographic feature size that is both less than 20% the size of the lithographically defined diameter and independent of variations in that larger hole diameter.

The keyhole-transfer process should scale well into future technology nodes. As the lithographically defined hole size becomes smaller, the amount of material through which the keyhole needs to be transferred [step 4 of Figure 6(a)] will simply become smaller because of the conformal nature of the film deposition [step 3 of Figure 6(a)]. Furthermore, this same keyhole-transfer process can also be used to construct a sublithographic-sized yet highly controlled bottom electrode for the mushroom cell.

Also under investigation is the utilization of a Ge nanowire as a bottom electrode for the mushroom cell [76]. This cell concept not only has the advantage that the bottom electrode size is controlled by the growth conditions of the nanowire, but also has the advantage that the n-type doped nanowire forms a diode at the connection to a p-type substrate and could potentially serve as the access device of the memory cell.

Summary and outlook

In this paper, we have analyzed the scaling behavior of PCRAM technology in terms of the expected device properties, the scaling properties of the phase-change materials themselves, the performance of actual ultrascaled prototype devices, and the fabrication challenges that can be expected at future technology nodes. Simulations indicate that the critical value of the RESET current will continue to shrink rapidly with the size of the phase-change memory element. We show that the properties of phase-change materials are generally conserved with films that have thicknesses as small as only 10 nm, depending somewhat on the material. For thinner films, an increase in the crystallization temperature is observed that makes these films even better suited for PCRAM applications. Nanoparticles as small as 15 nm have been fabricated and still show crystallization at temperatures that are comparable to bulk material for many cases. Functioning devices have been fabricated using films as thin as 3 nm, with cross-sectional areas of only 60 nm^2. Integration schemes have been developed that can potentially implement such sublithographic critical dimensions within the phase-change memory cell, even in the presence of significant device-to-device variations in the lithographic patterning. Thus, in many aspects, PCRAM technology appears to be readily scalable to several future technology nodes.

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