

Large-scale (512kbit) integration of Multilayer-ready Access-Devices based on Mixed-Ionic-Electronic-Conduction (MIEC) at 100% yield

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Abstract

BEOL-friendly Access Devices (AD) based on Cu-containing MIEC materials [1-4] are integrated in large (512×1024) arrays at 100% yield, and are successfully co-integrated together with Phase Change Memory (PCM). Numerous desirable attributes are demonstrated: the large currents ($>200\mu\text{A}$) needed for PCM, the bipolar operation required for high-performance RRAM, the single-target sputter deposition essential for high-volume manufacturing, and the ultra-low leakage ($< 10\text{ pA}$) and high voltage margin (1.5V) needed to enable large crosspoint arrays.

Keywords: Access device, MIEC, PCM, NVM, RRAM, MRAM

Introduction

For PCM, RRAM, MRAM, or any other nonvolatile memory (NVM) to be as cost-effective as NAND FLASH ($\leq 4F^2/3$), 3D-stacking of large crosspoint arrays in the BEOL will be essential. Previously [1,2], we have shown that MIEC-based ADs exhibit the large ON/OFF ratios that enable these large crosspoint arrays (Fig. 1), with high voltage margin V_m (for which leakage stays below 10 nA), ultra-low leakage ($< 10\text{ pA}$), and high enough current densities even for PCM. In addition, these devices show bipolar diode-like characteristics, making them uniquely suited for stacking high-density MRAM and RRAM in the BEOL.

MIEC AD demonstrations shown to date have been encouraging but at research-scale, with small (5×10) arrays of ADs integrated without any NVM. In this paper, we show that MIEC ADs support both processing temperatures up to 500°C and the single-target sputter deposition needed in manufacturing, and demonstrate process improvements that provide both lower leakage and wider voltage margins. Furthermore, we demonstrate small device arrays with co-integrated MIEC and PCM devices, as well as large-scale (512kbit) arrays of integrated MIEC ADs at 100% yield.

MIEC device fabrication and process improvements

All MIEC-based ADs presented here (Fig. 2) are integrated on 8" wafers, using sputter-deposition of Cu-containing MIEC material into vias followed by an optimized CMP process [2] and a confined, non-ionizable TEC (Fig. 2(a)). Short-loop devices (Fig. 2(b)) have minimal wiring and are tested with Conductive-AFM. While our multi-target-capable PVD tool has allowed us to easily fabricate different MIEC materials [2], short-loop devices deposited from a single target, as required for volume manufacturing, show near-identical device characteristics (Fig. 3). Cumulative post-fabrication anneals up to 500°C are also shown to have minimal effect on device yield, as measured over >1000 short-loop devices (Fig. 4), providing a wide processing window.

Process improvements developed in short-loop devices can be transferred to integrated 8" wafers containing small arrays of 180nm-node FETs (Fig. 2(c)). Fig. 5 illustrates the improvement in per-device leakage on an all-good array of 5×10 MIEC-based ADs after electrode optimization. While voltage margin V_m as measured at 10nA is effectively unchanged, the voltage windows at both 10pA and 100pA are markedly improved. Further process improvements have led to much larger voltage margins ($V_m=1.5\text{V}$), sufficient for PCM, RRAM, and MRAM (Fig. 6).

MIEC devices integrated with PCM

MIEC-based ADs were also integrated immediately above ring-electrode mushroom-cell (CD $\sim 35\text{nm}$) Phase-Change Mem-

ory devices (Fig. 2(d)), fabricated using the keyhole-transfer method [5]. When tested in small arrays (5×10) immediately after completion of M1 wiring (Fig. 7(a)), the large resistance change of PCM is readily evident above $\sim 500\text{mV}$. While three of the 50 MIEC ADs have higher leakage, the three associated PCM devices could be placed in a permanent high-resistance state (Fig. 7(b)) using reverse polarity pulses [6]. Thus singleton AD failures need not devastate future crosspoint array yield, at least with PCM. As shown in Fig. 8, endurance of integrated PCM+MIEC device pairs can exceed 100,000 cycles, despite the repeated application of RESET pulses $>200\mu\text{A}$ and $5\mu\text{s}$ long SET pulses at $\sim 90\mu\text{A}$.

Large MIEC device arrays at 100% yield

BEOL processing conditions (including temperatures and dielectrics) and AD electrodes were optimized for high array-yield and tight distributions. After optimized Cu-damascene M2 wiring (Fig. 2(d)), bi-directional Array Diagnostic Monitor (ADM) arrays up to 512×1024 integrated MIEC ADs could be tested using integrated 1-bit sense-amplifiers and a fast electrical tester (Magnum 2EV, Fig. 9). Cumulative distribution functions (CDFs) of the bit-line voltage V_{BL} needed to produce various device currents I_d can be combined to show the tightly distributed array I-V characteristics (Fig. 10). All 524,288 MIEC devices — 100% — had $V_m > 1.1\text{V}$, and 99.955% of ADs fell within $\pm 150\text{mV}$ of the median voltage margin $V_m=1.36\text{V}$ at 10nA (Fig. 11); these characteristics were uniform across the entire array (Fig. 12). In contrast, with the original, unoptimized electrode process, MIEC AD yield was significantly lower (91%), with numerous leaky devices and pronounced "edge effects" (Fig. 13).

MIEC and RRAM

While some RRAM devices can be made unipolar, large read-write voltage margins and high endurance has required bipolar operation. Being inherently bipolar-capable, MIEC-based ADs offer the best of a very few paths for combining high-performance bipolar RRAM with Multi-Layer stacking.

Conclusions

BEOL-friendly access devices (AD) based on copper-containing MIEC materials [1-4] uniquely enable Multi-Layer Crosspoint-Memory Arrays, offering the large currents ($>200\mu\text{A}$) needed for PCM, the bipolar operation required for high-performance RRAM, the single-target sputter deposition essential to high-volume manufacturing, and the ultra-low leakage ($< 10\text{ pA}$) and high voltage margin (1.5V) needed for large crosspoint arrays. MIEC ADs were co-integrated successfully in small arrays with PCM, and were integrated in large (512×1024) arrays with 100% yield.

Acknowledgements

Expert analytical and processing support from D. Pearson, E. Delenia, L. Krupp, A. Friz, and the Microelectronics Research Laboratory (YKT) is gratefully acknowledged.

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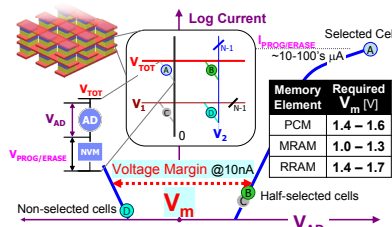


Fig. 1 In an NVM crosspoint array, the Access Device (AD) must supply high current for program/erase of a selected cell yet low-leakage for all other cells, including those half-selected. A voltage margin V_m of 1.5V would be sufficient for PCM, RRAM, and MRAM.

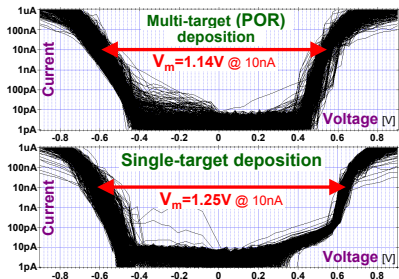


Fig. 3 Short-loop ADs show that Cu-containing MIEC material deposited from a single-target has identical (or even improved) I-V characteristics to our POR ADs (deposited from multiple targets).

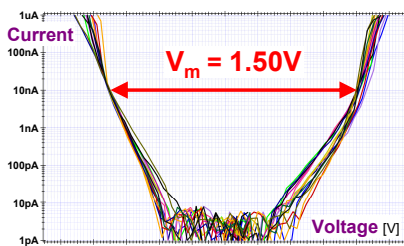


Fig. 6 I-V characteristics show voltage margins $V_m=1.50V$ (at 10nA) for short-loop ADs fabricated with extensive process improvements.

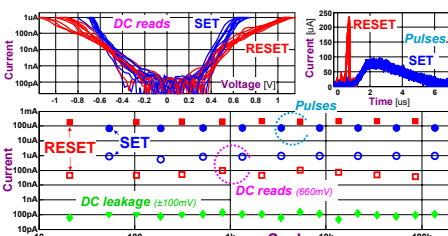


Fig. 8 Endurance of an integrated PCM+MIEC device-pair to >100k cycles, with RESET currents >200 μA and 5 μs -long SET pulses (~90 μA). No AD degradation had occurred at the time testing was terminated.

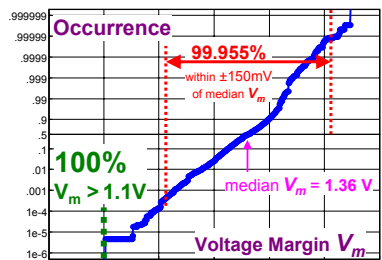


Fig. 11 Within this same 512 $\times$ 1024 array, there were no leaky devices; 100% of the array showed $V_m > 1.1V$. 99.955% of MIEC ADs had voltage margins V_m at 10nA within $\pm 150mV$ of the median of 1.36V.

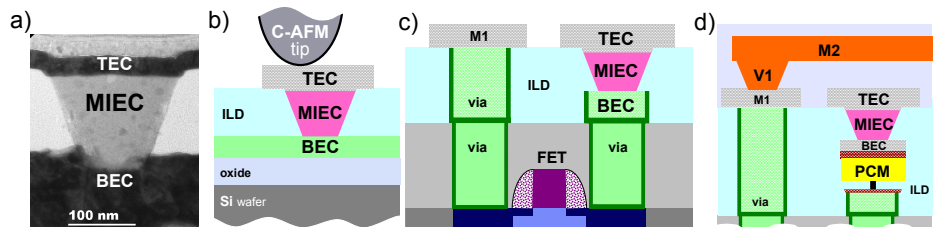


Fig. 2 MIEC-based ADs are integrated on 8" wafers, with MIEC material sputter-deposited into vias followed by an optimized CMP process[2] and a confined, non-ionizable TEC (a). Short-loop devices (b) have minimal wiring and are tested with Conductive-AFM, while integrated 180nm FETs allow (c) small (5 $\times$ 10) arrays of MIEC ADs to be tested. Mushroom-cell PCM devices with ~35nm CD heater electrodes (d) were integrated with the keyhole-transfer A method [5], followed by the MIEC AD. Completion of (d) dual-damascene copper M2 wiring allowed testing of large Array Diagnostic Monitor (ADM) arrays up to 512 $\times$ 1024 in size, either with or without PCM.

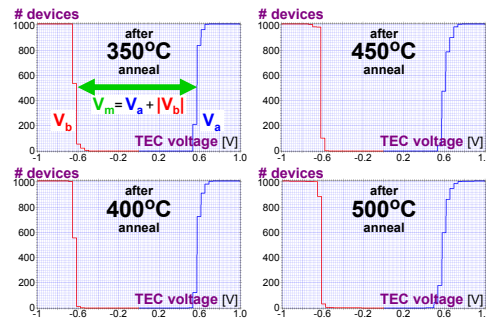


Fig. 4 Cumulative distributions of V_m over >1000 short-loop MIEC-based ADs after successive high-temperature anneals.

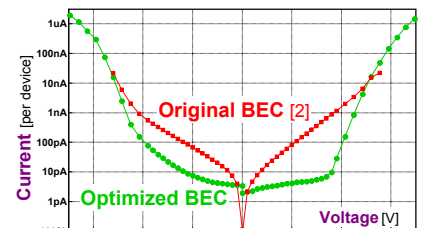


Fig. 5 Slow measurements on entire all-good arrays of ~50 integrated MIEC ADs reveal that already-low leakage currents can be further suppressed through electrode optimization.

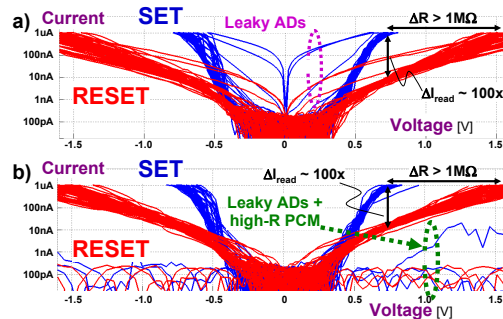


Fig. 7 a) I-V characteristics for a 5 $\times$ 10 macro of MIEC ADs stacked on PCM. Switching between SET and RESET does not degrade the ADs, but three ADs are noticeably leaky. Leaky ADs would adversely affect all device-pairs on the same row and column in any future crosspoint array; even a handful would greatly decrease array-yield. Reverse polarity pulses can intentionally damage only the PCM devices in series with leaky ADs [6], leaving those PCM+MIEC device pairs in a high resistance state (b) and eliminating the amplification effect of singleton AD failures.

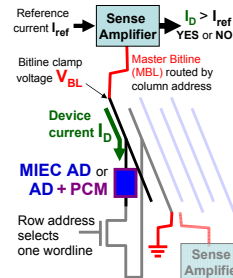


Fig. 9 Integrated 1-bit sense-amplifiers allow a fast electrical tester (Magnum 2EV) to bi-directionally query ADM devices.

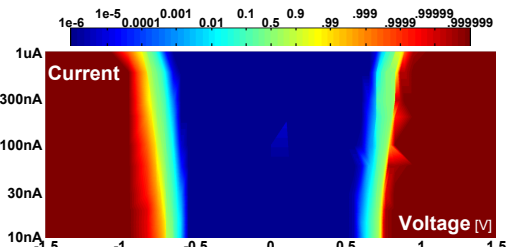


Fig. 10 Array level I-V results across a 512 $\times$ 1024 array of integrated MIEC ADs show tight distributions. Cumulative distribution functions (CDFs) across bitline voltage V_{BL} at various device currents I_d are combined; by using 1024 $\times$ 1024 addresses, all 512 $\times$ 1024 MIEC ADs can be addressed in both polarities.

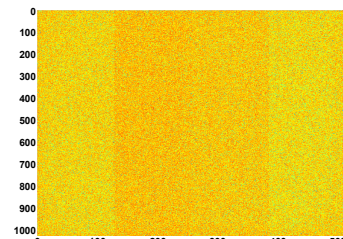


Fig. 12 After the BEOL processing conditions and AD electrodes were optimized, voltage margins V_m were uniformly distributed across the entire 512 $\times$ 1024 array of MIEC ADs, with no "edge effects."

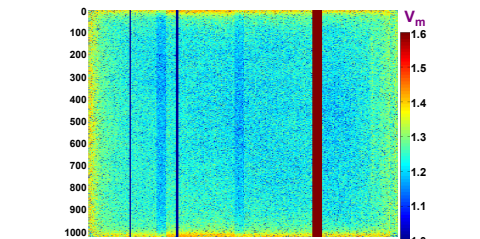


Fig. 13 In contrast, with the original, unoptimized process (on a 256 $\times$ 1024 array), MIEC AD yield was significantly lower (91%), with numerous leaky devices and pronounced "edge effects." The non-responsive bitlines seen here are not related to the MIEC process.