Highly-Scalable Novel Access Device based on Mixed Ionic Electronic Conduction (MIEC) Materials for High Density Phase Change Memory (PCM) Arrays

K. Gopalakrishnan, R. S. Shenoy, C. T. Rettner, K. Virwani, D. S. Bethune, R. M. Shelby, G. W. Burr, A. Kellock, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, B. Jackson, A. M. Friz, T. Topuria, P. M. Rice, and B. N. Kurdi

IBM Almaden Research Center, 650 Harry Road, San Jose, California 95120

Tel: (408) 927{–3721, –2362}, Fax: (408) 927–2100, E-mail: {*kailash, rsshenoy*}*@us.ibm.com*

Abstract

Phase change memory (PCM) could potentially achieve high density with large, 3D-stacked crosspoint arrays, but not without a BEOL-friendly access device (AD) that can provide high current densities and large ON/OFF ratios. We demonstrate a novel AD based on Cu-ion motion in novel Cu-containing Mixed Ionic Electronic Conduction (MIEC) materials[1, 2]. Experimental results on various device structures show that these ADs provide the ultra-high current densities needed for PCM, exhibit high ON/OFF ratios with excellent uniformity, are highly scalable, and are compatible with <400°C Back-End-Of-the-Line (BEOL) fabrication.

Keywords: Access device, Diode, MIEC, PCM, PCRAM

Introduction

PCM is a promising next-generation memory candidate because of its ease of integration, scalability, speed and endurance. But to be as cost-effective as NAND FLASH ($\leq 4F^2/3$), 3D-stacking of large crosspoint arrays in the BEOL will be necessary[3,4]. Fig. 1 shows calculated (mushroom-cell: ITRS) as well as experimental (our pore-cell) PCM RESET currents. The corresponding current densities (J ~5–20MA/cm^2) challenge amorphous or polycrystalline-Si p-n junctions. Large arrays improve array efficiency, but mandate an AD with large ON/OFF ratios ($\geq 10^7$).

Device structure and Method of operation

We have explored the use of novel Cu-containing MIEC materials as Access Devices uniquely suited to large, 3D PCM arrays. Fig. 2 shows a typical device structure, with MIEC material sandwiched between two electrodes (at least one must be inert or non-Cu-ionizing). These materials have a significant amount of mobile Cu, and negatively-charged vacancies behave like acceptor sites. Negative bias on the top electrode (TEC) pulls Cu^+ ions away from the bottom electrode (BEC). The increased acceptor (and hole) concentration near the BEC depends exponentially on the applied bias[1, 2], and results in a steady-state hole diffusion current due to the vertical gradient in hole concentration. The large fraction of mobile Cu enables very high current densities.

Experimental Results

The process flow used to build these devices is described in Fig. 3. An integrated polysilicon resistor is fabricated in series with every AD in order to measure the current flowing during high-speed pulsing. ADs were built by sputter-depositing MIEC and TEC materials into e-beam-defined vias (etched into SiN_x stopping on an inert BEC). Devices with different film thicknesses, dielectric thicknesses, TEC and BEC CDs, and inert vs. ionizable TECs were fabricated and measured. All relevant processing temperatures were kept <400°C. Fig. 4 shows a TEM of a 250nm BEC AD with a wide-area ($CD_{TEC} \gg CD_{BEC}$), ionizable TEC.

Fig. 5 shows superimposed i-v characteristics for sixty 80nm BEC devices with wide-area ionizable TECs. As predicted by MIEC theory, an exponential diode-like i-v (starting at voltage V_B) is seen when the TEC-to-BEC bias is negative. Device to device variability is minimal. For positive bias, exponential characteristics are preempted by an abrupt current increase (at V_A), as the vast number of ions swept from the wide-area TEC into the small via electrolytically form a reversible metallic filament. This interpretation is bolstered by data from symmetric MIEC lateral-bridge-cells connecting inert electrodes (Fig. 6). For symmetric devices with limited MIEC volume, electrolytic filaments do not form, and bipolar exponential characteristics are observed.

Pulsed characteristics for 40nm BEC devices are shown in Fig. 7. Currents exceeding 200 μA (J > 15 MA/cm^2) are readily obtained from these devices. The duration (few 100ns) and temperature dependence (inset of Fig. 7) of the turn-on transients confirm MIEC, rather than electronic-Schottky, behavior. AD performance after sequential pulses of low- and high-current is shown in Fig. 8, with series resistances chosen to emulate typical PCM read and write conditions. Endurance exceeding 10^{10} cycles (10^5 cycles) for low (high) currents have been obtained, with further optimization possible through pulse shaping.

The impact of BEC scaling (for wide-area, ionizable TECs) is shown in Fig. 9. Perfect scaling of current with BEC area is observed from 1μm down to 40nm BEC diameter. Ultra-scaled (19nm BEC) devices can support extremely high current densities (>50 MA/cm^2, inset of Fig. 9), although they non-destructively turn themselves OFF in approximately 200ns (more than sufficient to RESET PCM). Preliminary results on PCM+AD operation are shown in Fig. 10, using a test structure (inset) that allowed independent probing of the PCM, the AD (fabricated post-PCM process) and their series combination. The 34nm pore-cell PCM was successfully cycled through $>3 \times 10^4$ SET-RESET cycles, with no degradation observed in any characteristics of the nearby 80nm AD that supplied all PCM-read and -write currents.

While these results demonstrate the high current densities and low-temperature-compatible processing required for stacked PCM arrays, the turn-on voltages V_A and V_B of these wide-area ionizable TEC ADs (Fig. 5) are too low to support large-sized arrays without excessive half-select leakage. Fig. 11 indicates that, assuming bipolar array biasing, large arrays ($> 1024 \times 1024$) require only optimization of the PCM SET and dynamic resistances and higher AD voltage margin ($|V_A| + |V_B| > 1.0$V). As shown in Fig.12(a), we have successfully achieved such a large-array-capable AD device by combining process optimization with the scaling of inert TECs down to <400nm CD. These devices show symmetric bipolar-exponential characteristics, with no electrolytic filament. As predicted by MIEC theory, the lower concentration of ions increases $|V_B|$ so that voltage margins >1V are obtained with ~200nm TEC CDs (Fig. 12(b)) without sacrificing high current-density.

Conclusions

Novel Access Devices based on MIEC materials can be fabricated at <400°C, are extremely scalable, and can conduct very high current densities — making them highly interesting for stacking of multi-layer PCM arrays in the BEOL. These ADs require no breakdown, allowing truly non-destructive PCM reads, and hold the potential for combining multi-level cells (MLC) together with 3D stacking. The large voltage margins essential for large arrays have been demonstrated by combining MIEC materials and AD process optimization with a scaled inert TEC.

Acknowledgements

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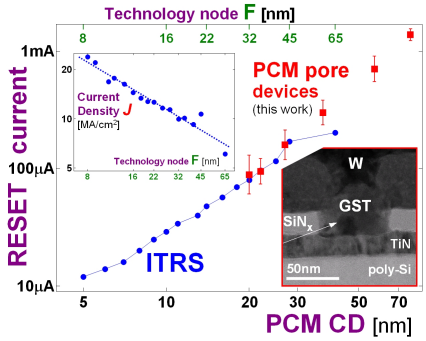

Fig. 1 RESET current of PCM pore devices (inset: CD∼50nm) as a function of CD and technology node, compared to ITRS[5]. Inset: expected current density, J, in an AD of diameter F.

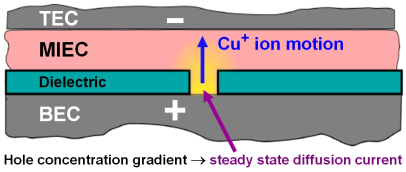

Fig. 2 Negative bias on the TEC pulls Cu^+ ions away from the BEC, leaving vacancies that act as acceptors. Electrochemistry induces a gradient in hole density, exponentially dependent on bias, which then drives steady-state hole current. Large current densities are possible because the fraction of displaceable Cu atoms is high.

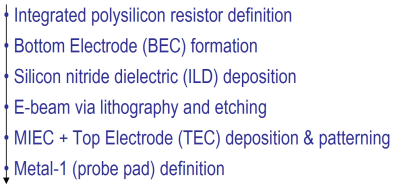

Fig. 3 Flowchart of key steps in the process integration for fabricating novel AD test structures and integrated polysilicon resistors (used to measure pulse current). The BEC and all subsequent materials are PVD-deposited, and are processed at temperatures $<400°$C.

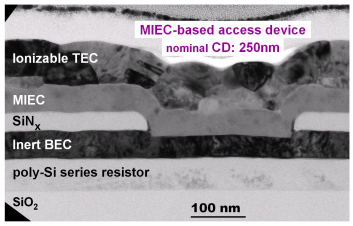

Fig. 4 Cross-sectional TEM of MIEC-based AD with a wide-area ionizable TEC. The MIEC material fills an approximately 250nm sized via etched into silicon nitride (typically 40nm thick), stopping on the inert bottom electrical contact (BEC).

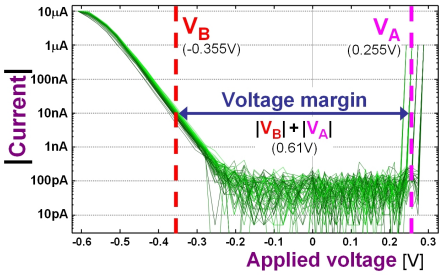

Fig. 5 Superimposed i-v characteristics of sixty MIEC devices (80nm BEC, wide-area ionizable TEC). Negative bias on the TEC produces very tight, exponential diode-like i-v characteristics. At moderate positive bias, Cu^+ ions swept from the large TEC into the tiny via form a metallic filament and current abruptly increases.

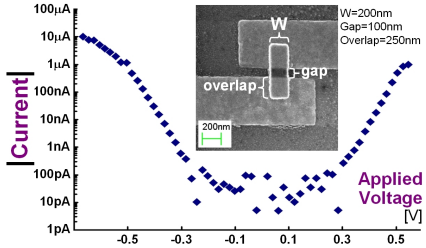

Fig. 6 Results for a lateral MIEC bridge device with fully symmetric, non-ionizable electrodes. As expected, symmetric devices with non-ionizable TECs show symmetric exponential characteristics with no abrupt electrolytic turn-on. While back-to-back electronic-Schottky diodes would produce only leakage currents, no significant current reduction is seen in MIEC devices.

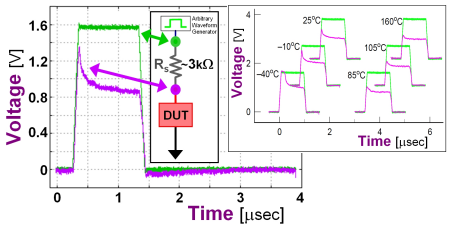

Fig. 7 Pulsed characteristics of an AD (40 nm BEC, wide-area ionizable TEC) in series with an integrated polysilicon resistor (3kΩ). At 1.6V bias, currents >200 μA are readily obtained, even in 40nm devices ($\boldsymbol{J > 15}$ **MA/cm²**). Inset: pulsed AD characteristics as a function of temperature. Current build-up requires ∼100ns depending on temperature, MIEC thickness, and other parameters.

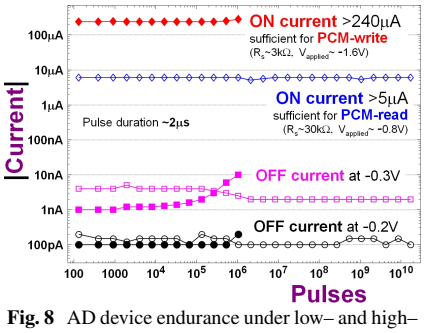

Fig. 8 AD device endurance under low– and high–current conditions. Low-voltage DC measurements show low OFF current despite $> 10^{10}$ low-current pulses. While OFF current increases $10\times$ (∼60mV shift in i-v curves) after $\sim 10^6$ high-current cycles, pulse-shaping allows further optimization.

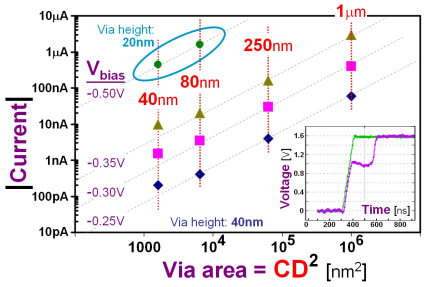

Fig. 9 Current in AD devices with ionizable, wide-area TECs scales perfectly with BEC area. Here 40nm vias are defined in thinner (20nm rather than 40nm thick) dielectric to finesse limits of sputter deposition. Inset: ultrasmall (19nm) AD with ionizable, wide-area TEC defined in thin (13nm) dielectric passes currents >165 uA ($\boldsymbol{J > 50}$ **MA/cm²**).

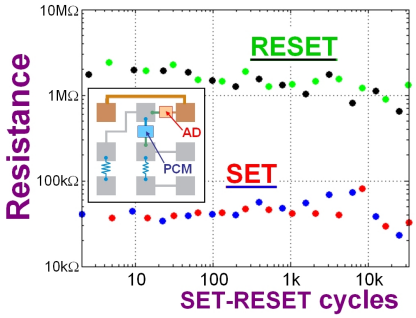

Fig. 10 Cycling of a 34nm pore-cell PCM, with SET, RESET, and read performed through a nearby 80nm AD. While the PCM resistances show a slight downward trend, the AD shows no degradation over $> 3 \times 10^4$ cycles. Inset: test structure used to allow independent access to PCM, co-integrated AD, and combined PCM+AD device.

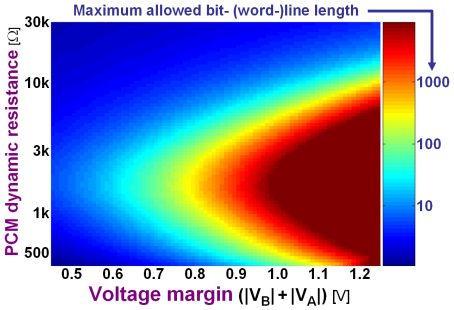

Fig. 11 Predicted maximum size of a memory array, under bipolar biasing, allowed by leakage constraints as a function of PCM dynamic resistance and AD voltage margin. Voltage margin exceeding 1.1V is needed for high array-efficiency.

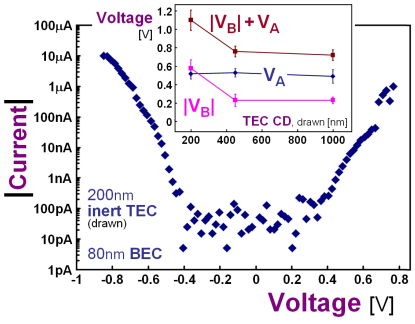

Fig. 12 Device results for process-optimized AD with non-ionizable scaled TEC. As the TEC is scaled below 450 nm, the electrolytic abrupt turn-on is replaced by exponential i-v behavior, and (inset:) turn-ON voltage $|V_B|$ increases significantly (possibly because of lower total ion concentration). Thus voltage margins >1.0V are easily obtained at TEC CDs ∼200nm.