Sub-30nm scaling and high-speed operation of fully-confined Access-Devices for 3D crosspoint memory based on Mixed-Ionic-Electronic-Conduction (MIEC) Materials

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Abstract

BEOL-friendly Access Devices (AD) based on Cu-containing MIEC materials [1-3] are shown to scale to the <30nm CDs and <12nm thicknesses found in advanced technology nodes. Switching speeds at the high (>100uA) currents of NVM writes can reach 15ns; NVM reads at typical (∼5uA) current levels can be ≪1usec.

Introduction

Making PCM, RRAM, MRAM, or any other nonvolatile memory (NVM) as cost-effective as NAND FLASH ($\leq 4F^2/3$) will require 3D-stacking of large crosspoint arrays in the BEOL. Previously [1–3], we have shown (Fig. 1) that MIEC-based ADs exhibit the large ON/OFF ratios needed for large crosspoint arrays, with bipolar diode-like characteristics, large voltage margin V_m (for which leakage stays below 10 nA), ultra-low leakage (< 10 pA), and high ON current densities. 512kBit arrays of such MIEC ADs have been integrated with 100% yield (Fig. 1(b)) [3].

While early MIEC ADs had ultra-scaled bottom electrodes (BEC < 20nm), top electrodes (TEC) were much larger [1]. Later demonstrations of moderate-aspect-ratio, confined MIEC ADs have used CDs from 80–180nm [2–3], and operation speed was only briefly investigated [1]. In this paper, we address write speed by demonstrating rapid (15ns) PCM RESET, evaluate the prospective read speed of MIEC ADs at lower currents with an array-integrated Sense Amplifier, and use short-loop MIEC devices to aggressively scale both thickness and critical dimension (CD).

Speed of MIEC ADs for NVM write and read

To demonstrate NVM write speed capabilities, an MIEC-based AD was used to rapidly RESET a co-integrated phase change memory (PCM) device (Figs. 2,3). Between each 15ns RESET pulse at varying amplitude (Fig. 4(a)), a long SET pulse (Fig. 4(b)) was used to recrystallize the doped-$Ge_2Sb_2Te_5$ PCM material. After each pulse, bipolar dc IV curves were measured (Fig. 5), to gauge

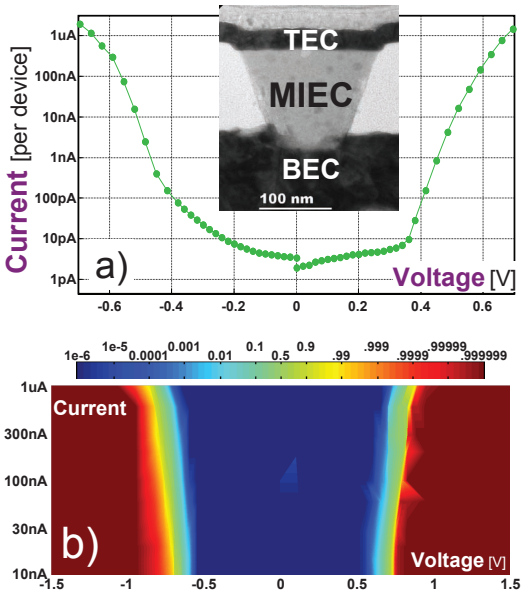

Fig. 1 MIEC-based ADs exhibit the large ON/OFF ratios needed for large crosspoint arrays, showing high voltage margin V_m (for which leakage stays below 10 nA), high ON current densities [1], (a) ultra-low leakage (< 10 pA) [2,3], and (b) tight margins (as well as 100% yield) when integrated on 8" CMOS wafers in large (512kBit) arrays [3].

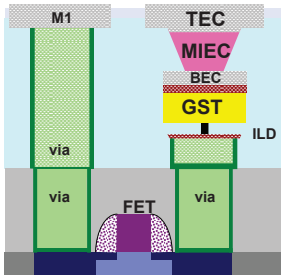

Fig. 2 MIEC-based ADs are co-integrated with PCM and a 180nm FET.

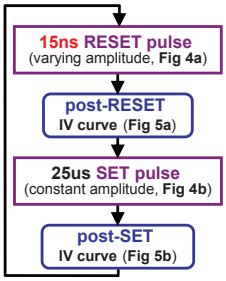

Fig. 3 Switching of PCM with a MIEC-based AD alternated between 15ns RESET pulses at varying amplitude, a long SET pulse, and dc IV curves.

both the resistance state and the low-leakage characteristics of the MIEC AD. Read current at 660mV (Fig. 6) reveals full switching after single RESET pulses, demonstrating that MIEC-based ADs can supply ∼200uA in <15ns.

At the much lower (5–10uA) current levels associated with NVM reads, the pulsed response of small-array integrated MIEC ADs (Fig. 7) can become difficult to unambiguously distinguish from background noise. While signal strength can be greatly increased by measuring multiple MIEC ADs in parallel, the increased parasitics and presence of unequal current division (even for slight device-to-device variations) also introduce significant uncertainty.

However, we can accurately measure such currents with the sense amplifier (SA) integrated with our large (512kBit) arrays. Although the SA has its own temporal response, we can isolate this with nearby ROM arrays integrated with polysilicon resistors, and then compare the slower response of integrated MIEC ADs through the same type of SA (Fig. 8). Fig. 9 combines data from the high-current measurements (Fig. 4(a)) with these indirect measurements using the large-array SA to illustrate the highly nonlinear turn-on of MIEC devices. Although full saturation of MIEC ADs at the typical read current levels expected for future NVM reads (∼5uA) is not rapid, either the application of shaped pulses (Fig. 10) or a transient "overvoltage" read (green dashed circle in Fig. 8) can readily allow ∼5uA NVM reads in ≪1usec using MIEC ADs.

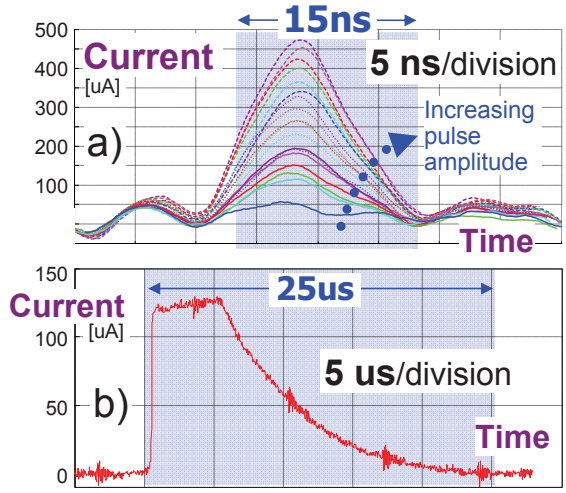

Fig. 4 Since melting can be initiated very rapidly, PCM RESET occurs as rapidly as the co-integrated MIEC AD can supply sufficient switching current; in contrast, SET speed is limited by crystallization of the doped $Ge_2Sb_2Te_5$ (GST).

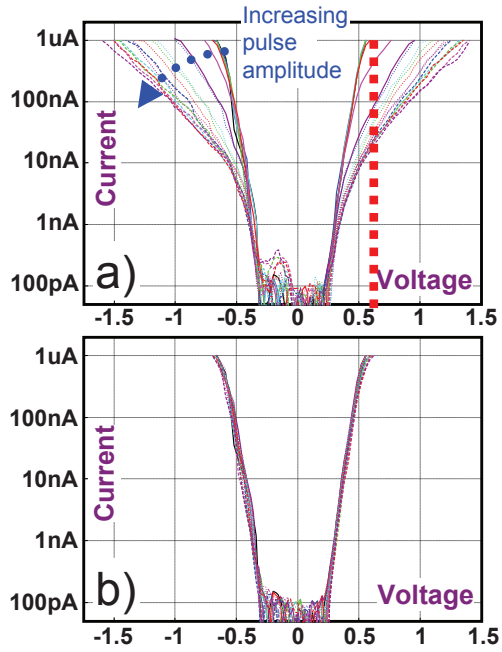

Fig. 5 After each RESET or SET pulse (Fig. 4), bipolar dc IV curves were measured. Once the current supplied by MIEC is sufficient to melt the GST, a large resistance contrast (∼1MΩ) between SET and RESET develops, associated with a significant change in the IV characteristics of the stacked device-pair. Despite the large currents, the low-leakage characteristics of the MIEC AD remain unaffected.

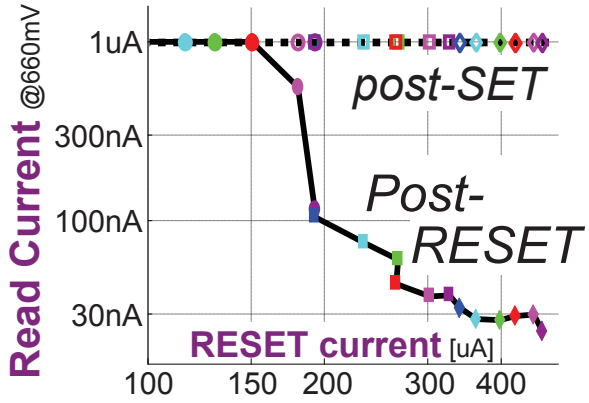

Fig. 6 Read current at 660mV shows full switching after single RESET pulses, demonstrating clearly that MIEC-based ADs can supply ∼200uA in <15ns.

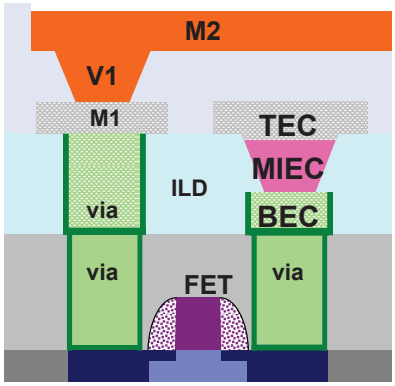

Fig. 7 MIEC ADs integrated with 180nm FETs and finished with M2 wiring can be tested in large arrays through an integrated 1-bit Sense Amplifier (SA).

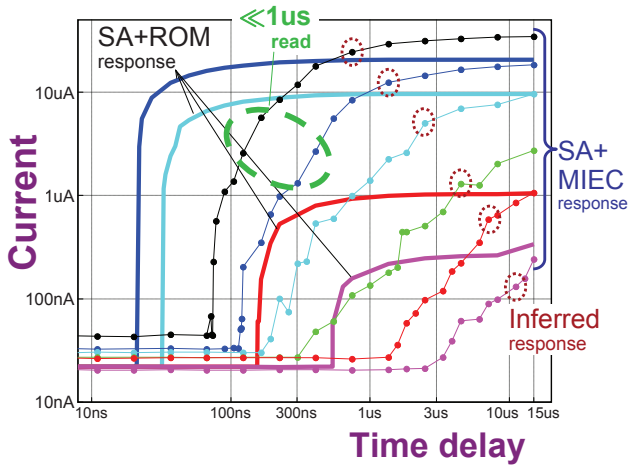

Fig. 8 To reliably measure the temporal response of MIEC ADs at low current, the selected wordline is enabled shortly before the Sense Amplifier (SA) state is latched, but after the SA has otherwise stabilized on the selected bitline. Nearby ROM arrays integrated with polysilicon resistors illustrate that a brief initial portion of this response is due to the internal dynamics of the SA, with the remainder due to the MIEC AD.

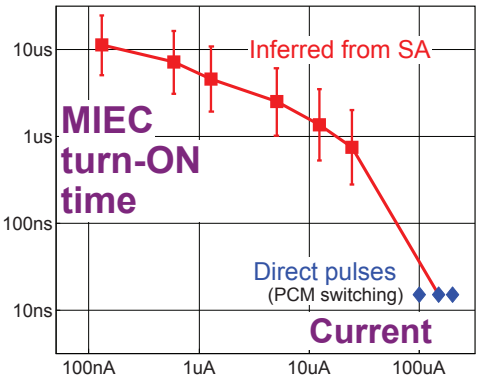

Fig. 9 Inferred temporal response of MIEC ADs, combining data from direct and precise high-current measurements (Fig.4(a)) and indirect measurements using the large-array SA.

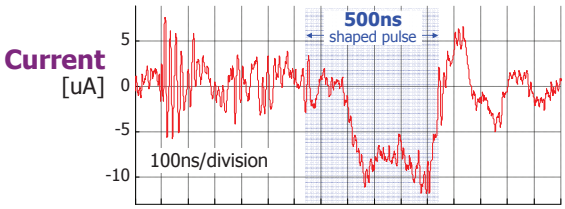

Fig. 10 Application of a shaped voltage pulse directly to an integrated (small-array) MIEC AD shows that ∼5uA currents suitable for NVM can be obtained in <1usec. Further use of "overvoltage" during MIEC AD turn-ON can be used to enable NVM read speeds ≪1usec, as demonstrated in the green dashed circle in Fig. 8.

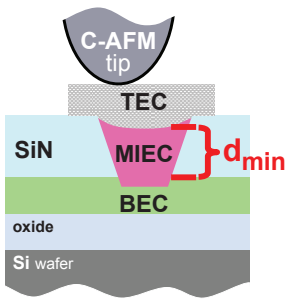

Fig. 11 Short-loop MIEC devices were fabricated with thinner SiN and/or smaller via diameters, and then tested with C-AFM.

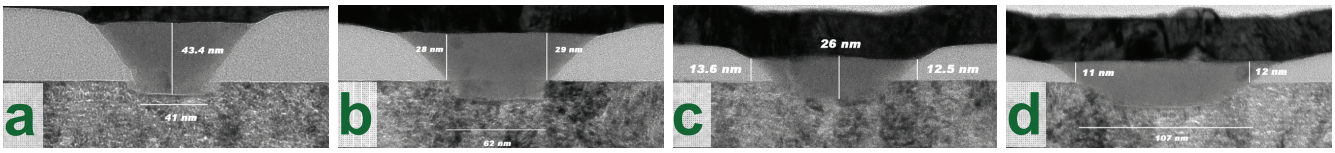

Fig. 12 Transmission Electron Micrographs (TEMs) of four representative devices with scaled SiN thicknesses. Due to over-etch into the BEC during via formation combined with dishing during CMP, the minimum device thickness d_{min} is located at the edge of the MIEC AD.

Thickness and CD scaling of MIEC ADs

By varying the thickness of SiN into which Cu-containing MIEC material was deposited [2], thickness scaling experiments were performed on short-loop devices tested with Conductive-AFM (C-AFM, Fig. 11). Over-etch into the BEC during via formation and dishing during Chemical-Mechanical Planarization (CMP) causes the minimum device thickness d_{min} (at the edge of the MIEC AD) to differ from (yet track with) the SiN thickness. As devices become thinner (Fig. 12), the distribution of voltage margins remains mostly unchanged (Fig. 13) until $d_{min} \sim$ 11nm (Figs.12,13(d)). Fig.14 shows a topographic AFM image and yield map of devices with an average $d_{min} \sim$ 12nm. Fig. 15 shows IV characteristics for the four neighboring devices marked in Fig. 14. Since the markedly leaky device with lower V_m (at 10nA) corresponds to $d_{min} \sim$ 6.0nm (Fig. 16), both yield and voltage margin appear insensitive to thickness down to $d_{min} \sim$ 11nm.

By using the keyhole-transfer method [4], short-loop MIEC ADs were fabricated with ultra-scaled vias. C-AFM testing of >1000 devices reveals high yield of devices with high voltage margin (median V_m >1.50V at 10nA, Fig. 17). Scaled (TEC CD $\sim$ 35nm) short-loop MIEC ADs, fabricated with the same MIEC material and tested with the same C-AFM methodology as larger (TEC CD $\sim$ 73nm) ADs (Fig. 18), exhibit a significant increase in V_m (from 1.25V to 1.60V), simply from CD scaling. Despite their small size, these MIEC ADs can still rapidly drive the large currents needed for NVM switching (Fig.19). Even more aggressively-scaled MIEC ADs retain all requisite characteristics,

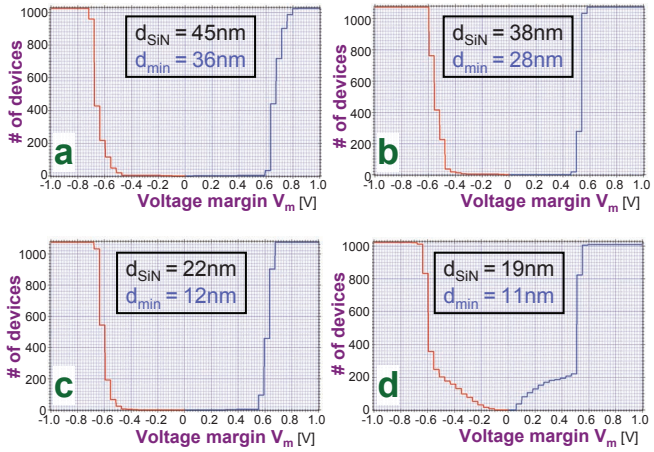

Fig. 13 Cumulative distribution functions (CDFs) of measured V_m at 10nA of >1000 MIEC ADs corresponding to the representative devices shown in Fig.12. As devices become thinner, voltage margins remain mostly unchanged until $d_{min} \sim$ 11nm (part (d)).

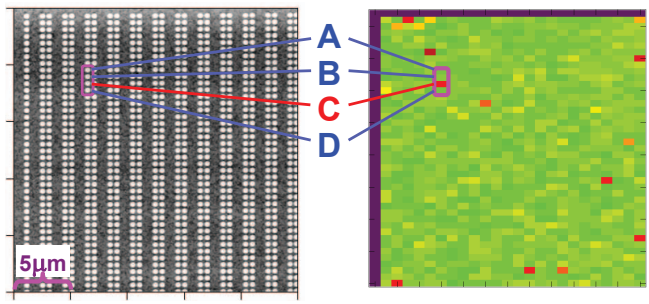

Fig. 14 Topographic AFM image and yield map for MIEC AD devices with an average $d_{min} \sim$ 12nm (Figs. 12, 13(c)). Four neighboring devices (indicated in magenta) were cross-sectioned for TEM.

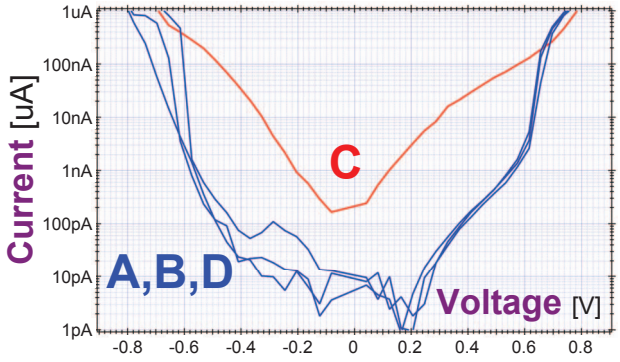

Fig. 15 IV characteristics for the four neighboring MIEC ADs marked in Fig. 14, showing three healthy MIEC ADs and one more leaky device with lower V_m.

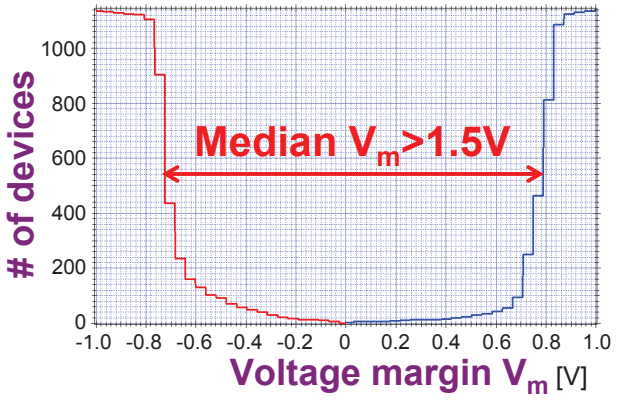

Fig. 17 Short-loop MIEC ADs fabricated with the keyhole-transfer method show a tight distribution of voltage margin V_m (at 10nA) about 1.50V and high yield.

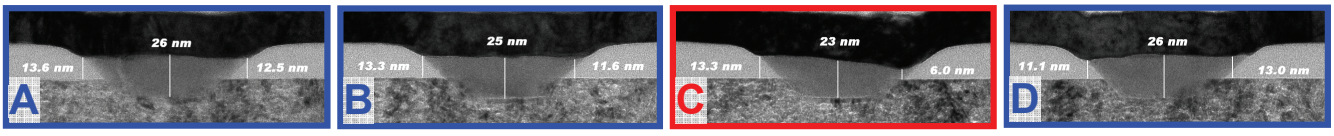

Fig. 16 TEMs of the marked MIEC ADs (Fig. 14) show that the markedly leaky device (Fig. 15(C)) corresponds to $d_{min} \sim$ 6.0nm. Devices with $d_{min} \sim$ 11.1–12.5nm exhibit similar low leakage and voltage margin characteristics as much thicker devices (Figs. 12,13).

including ultra-low leakage (<10pA) and the large voltage margins (V_m > 1.50V) needed for large arrays (Fig.20), despite having both top and bottom CDs <30nm (Fig. 21).

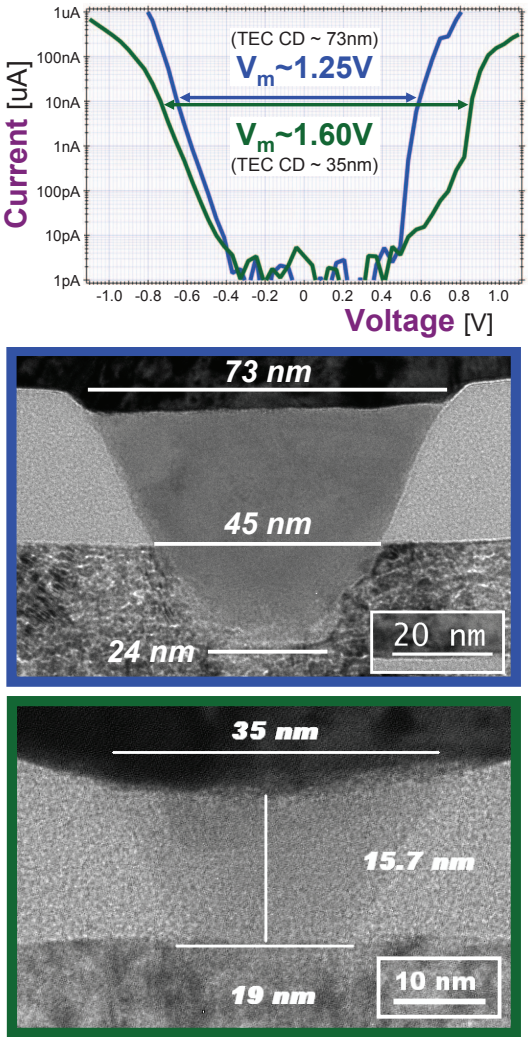

Fig. 18 IV characteristics of two short-loop MIEC ADs show the improvement in voltage margin V_m at 10nA (from 1.25V to 1.60V) made possible by CD scaling (from 73nm to 35nm).

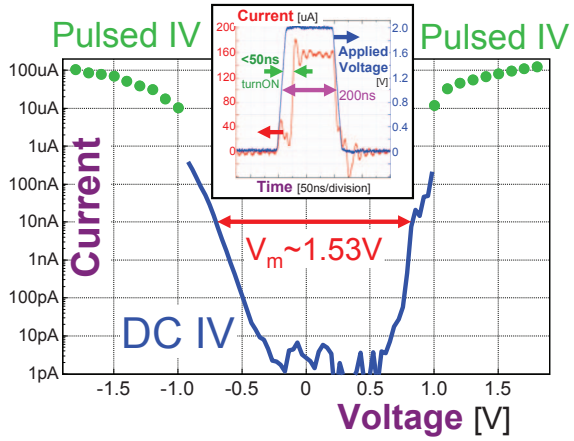

Fig. 19 In addition to high yield, scaled short-loop MIEC ADs exhibit the same >1e7 ON-OFF contrast, <50ns turn-ON times (test-setup-limited), and ultra-low leakage shown previously[2,3] in larger devices.

Conclusions

BEOL-friendly access devices (AD) based on copper-containing MIEC materials [1-4] uniquely enable Multi-Layer Crosspoint-Memory Arrays, offering the large currents (>100uA) needed for PCM and the bipolar operation required for high-performance RRAM. Despite the role of ionic motion, transient operation at >100uA (corresponding to NVM writes) is shown at 15ns; operation at ~ 5uA (corresponding to NVM reads) is demonstrated at ≪1us. Device thickness scaling down to a minimum thickness d_{min} ~ 11nm, and CD scaling down to <30nm CD (both TEC and BEC), are demonstrated. Voltage margin V_m (at 10nA) improves markedly as devices are scaled in lateral size. While leakage increases sharply for d_{min} ~ 6nm, **no lower limit to CD scaling has yet been identified**. Thus MIEC-based ADs are well-suited for both the scaled CDs and thicknesses of advanced technology nodes and the fast read and write speeds of emerging NVM devices.

Acknowledgements

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References

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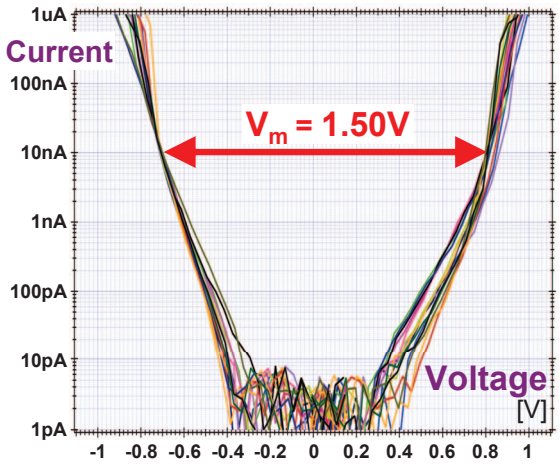

Fig. 20 Even more aggressively-scaled short-loop MIEC ADs[3] show large voltage margins and ultra-low leakage.

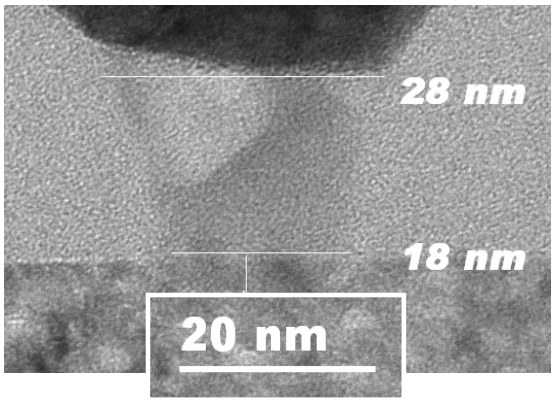

Fig. 21 Ultra-scaled MIEC ADs with both TEC and BEC <30nm, corresponding to the IV characteristics shown in Ref [3] and Fig.20.