Exploring the Design Space for Resistive Nonvolatile Memory Crossbar Arrays with Mixed Ionic-Electronic-Conduction (MIEC)–based Access Devices

P. Narayanan, G. W. Burr, R. S. Shenoy, S. Stephens, K. Virwani, A. Padilla, B. Kurdi, and K. Gopalakrishnan‡

IBM Research – Almaden, 650 Harry Road, San Jose, CA 95120 (‡IBM T. J. Watson Research Center, Yorktown Heights, NY 10598)
Tel: (408) 927–2920, Fax: (408) 927–2100, E-mail: *pnaraya@us.ibm.com*

Abstract

Using circuit-level SPICE simulations, we explore the design constraints on crossbar arrays composed of a nonvolatile memory (NVM) (+1R) and a highly nonlinear Access Device (AD) enabled by Cu-containing Mixed Ionic-Electronic Conduction (MIEC) materials [1-5]. Such ADs must maintain ultra-low leakage through a large number of unselected and partially selected 1AD+1R cells, while delivering high currents to the few cells selected for either read or write. We show that power consumption during write, not read margin, is the most stringent constraint for large 1AD+1R crossbar arrays, with NVM switching voltage V_{NVM} and selector voltage margin V_m being much more critical than write current. We show that scaled MIEC devices ($V_m \sim 1.54$V [4]) can support 1Mb arrays for V_{NVM} up to 1.2V. Stacking two MIEC devices enables $V_{NVM} \sim 2.4V$. A 20% improvement in V_m can either enable a 4× increase in array size or counteract a 5× increase in interconnect line resistance.

Keywords: Access device, MIEC, crossbar array, NVM selectors

Introduction

MIEC-based ADs [1–5] exhibit ideal characteristics for 3D-stacking of large crossbar arrays of any resistive NVM in the BEOL, including bipolar diode-like characteristics (Fig. 1), large ON/OFF ratios, high voltage margin V_m (for which leakage stays below 10 nA), ultra-low leakage (< 10 pA), and high ON current densities. Even with such attractive characteristics, however, the design of a large crossbar array of 1AD+1R devices (Fig. 2) — within which writes and reads must be reliable yet leakage through non-selected devices low — requires careful choice of selected & unselected wordline (V_W & V_R) and bitline (V_B & V_C) voltages. We quantify the design-space enabled by scaled MIEC-based ADs ($V_m \sim 1.54$V [4]) in terms of achievable array size, excess required power during write, and read margin.

Simulation framework

We assume an NVM device that transitions between an ohmic Low Resistance State (LRS) and a High Resistance State (HRS) exhibiting Poole-Frenkel (PF) conduction (Fig. 3). The equivalent circuit for the MIEC AD (Fig. 3, inset) is carefully fit to experimental data (Fig. 1). Before each SPICE simulation, the inner voltages V_C, V_R (Fig. 4(b)) are chosen for an aggregate unselected leakage of 10uA (e.g., for a 1Mb array, 10pA/device). As outer voltages V_B, V_W are swept apart, the voltage across the worst-case selected 1AD+1R device(s) (Fig. 4(a)) increases. After the simulation completes, the NVM switching event (Fig. 5) identifies the external voltages (V_B, V_W) required for a successful write. Default NVM, MIEC AD, and array parameters are shown in Table. 1. Total required power is examined just before and just after switching for both the LRS-to-HRS and HRS-to-LRS transitions.

Design space for NVM write

In our approach, only voltage choices which trigger a successful write are even considered. A design point becomes unfavorable when the total applied power becomes much larger than the base 1AD+1R write power. For instance, even a 10% increase in V_{HRS} causes applied power to increase by two orders of magnitude (Fig. 6). This extra applied voltage at the far-edge selected device (Fig. 4(a)) exponentially increases leakage in nearby half-selected devices (Fig. 4(b)). The resulting larger voltage drops in the wiring then exacerbate voltage stress at near-edge half-selected devices. While this positive feedback effect is roughly the same for the worst-case (all LRS) and for random stored data patterns, it can be suppressed by the high resistance of the HRS state (Fig. 6, inset). Like V_{HRS}, there is a V_{LRS} threshold, beyond which write power grows dramatically. However, the array design is quite robust to increases in switching currents I_{HRS}, I_{LRS} (Fig. 6).

Fig. 7 shows that small increases in V_{HRS} dramatically reduce achievable array size. When the design works (blue region at left), almost all the externally applied power reaches the selected device, opening up opportunities for parallel writes; when the design fails, almost all external power is dissipated in half-selected 1AD+1R devices. Figs. 8 and 9 show that, similar to NVM voltage V_{HRS}, maintaining a sufficiently large AD voltage margin V_m is critical to successful array design. Degradations in AD slope S lead to excess power (Fig. 8), yet can be offset by V_m improvements (Fig. 9).

For a given NVM, improvements in either the slope S or the voltage margin V_m of the MIEC-based AD can enable significant increases in the achievable array size (Fig. 10), or can be used to accommodate the increases in line resistances expected at scaled technology nodes (Fig. 11). Fig. 12 shows the achievable array size for both the scaled MIEC AD ($V_m \sim 1.54$V) and a stacked combination of two MIEC ADs. The larger voltage margin far outweighs the degradation in AD slope and series resistance, allowing a stacked MIEC diode to support 1Mb arrays for NVM switching voltages as large as 2.4V. Note that large SPICE simulations are enabled by modeling all unselected 1AD+1R device pairs with a single aggregate device (Fig. 13).

Design space for NVM read

Read margin is the change in voltage across a peripheral load resistor R_{LOAD} (Fig. 13) when the selected device moves between the HRS and LRS states. The applied read voltage is determined based on avoiding a disturb (Fig. 13(A)) on the near-edge cell, the two reads are performed with a true V/2 scheme and data patterns shown in Fig. 13(B,C)) (other schemes/patterns showed similar performance, not shown). The load resistance is chosen to increase read margin (Fig. 14, inset) without excessive RC timing issues. While read margin degrades with lower read voltage/disturb condition (Fig. 14), and higher interconnect resistance (Fig. 15, inset), NVM resistance contrast has the most significant impact (Fig. 15). Read margin does depend upon AD parameters (Fig. 16), but write power considerations are clearly far more stringent (Figs. 8,9).

Conclusions

We have explored the design of 1AD+1R crossbar arrays using highly nonlinear Access Devices (AD) based on Mixed Ionic-Electronic Conduction (MIEC) [1-5]. Circuit-level SPICE simulations were used to show that achievable array size and excess required power during write depends strongly on careful matching between the turn-on voltage V_m of the AD and the switching voltage V_{NVM} of the NVM. This implies that research in this field should be directed towards NVMs with lower V_{NVM} (and ADs with higher V_m), as opposed to decreases in raw NVM switching current. Scaled MIEC devices ($V_m \sim 1.54$V [4]) are shown to support V_{NVM} up to 1.2V (for 1Mb arrays), and two stacked MIEC devices enable $V_{NVM} \sim 2.4V$.

References

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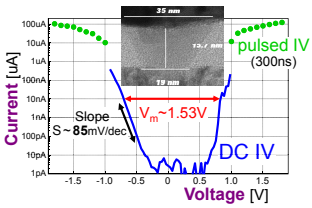

Fig. 1 Scaled MIEC access devices exhibit voltage margins V_m (at 10nA) of ~1.54V, ON-OFF contrast in excess of 10^7 and ultra-low leakage at low bias [1-5], suitable for large arrays with many unselected devices.

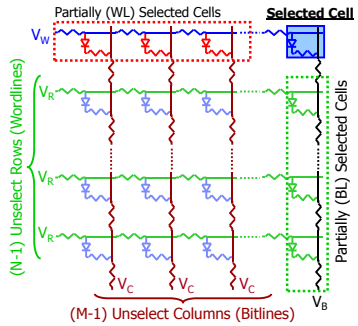

Fig. 2 Crossbar array with selected, partially (WL) selected, partially (BL) selected, and unselected 1AD+1R cells.

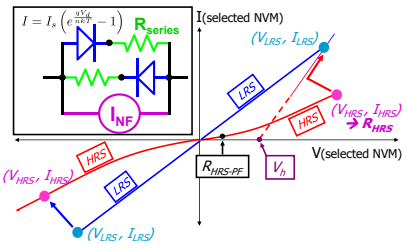

Fig. 3 Generic NVM model for SPICE, with switching between an ohmic LRS and an HRS exhibiting Poole-Frenkel conduction. Inset shows equivalent circuit for SPICE modeling of the bipolar, highly non-linear MIEC AD.

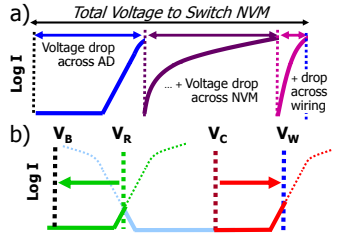

Fig. 4 Total applied voltage at switching is a) NVM voltage V_{NVM} + AD voltage + wiring IR-drop, identified by b) sweeping select-lines V_W and V_B at fixed unselect bias (and leakage).

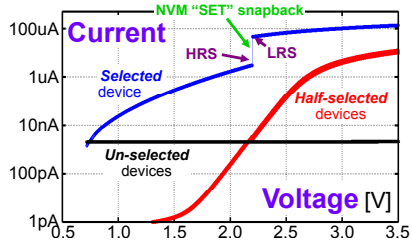

Fig. 5 Cell currents vs. total applied voltage for the HRS-to-LRS ("SET") operation on a 64×64 array, exhibiting NVM transition.

SET Switching	V_{HRS}, I_{HRS}	1.2V, 3μA
RESET Switching	V_{LRS}, I_{LRS}	0.8V, 30μA
Holding V during SET	V_h	0.5V
Read Disturb Voltage	V_{DIS}	0.25×V_{HRS}
Resistance States	R_{LRS}, R_{HRS}	26.67kΩ, 400kΩ
PF HRS @ 0.1V	R_{HRS-PF}	10MΩ
Voltage Margin	V_m	1.54V
Turn-on Slope	S	85mV/dec
Series Resistance	R_s	2850Ω
Noise Floor	I_{NF}	3pA
Array Size	$N \times M$	1Mb (1024×1024)
Interconnect R/cell[6]	R_{int}	2.215Ω

Table. 1 Default simulation parameters.

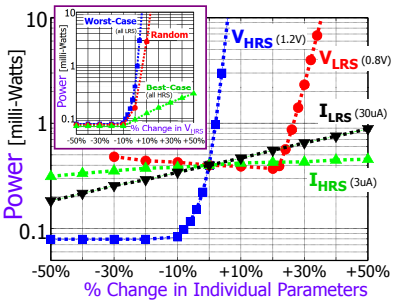

Fig. 6 Switching voltages (V_{HRS}, V_{LRS}) are much more critical to low power 1AD+1R crossbar design than switching currents (I_{HRS}, I_{LRS}). Inset: impact of data patterns.

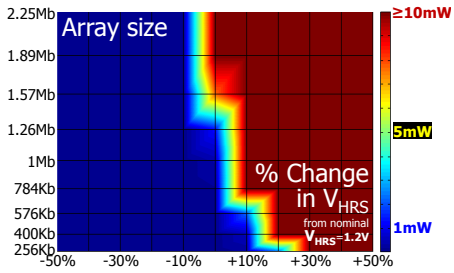

Fig. 7 Write power vs. V_{HRS} and array size: small changes in V_{HRS} dramatically reduce achievable array size.

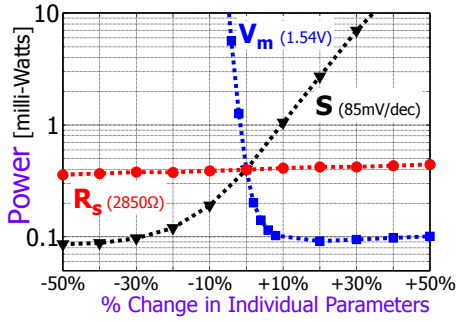

Fig. 8 Voltage margin V_m (at 10nA) is the most critical AD parameter in 1AD+1R crossbar Design.

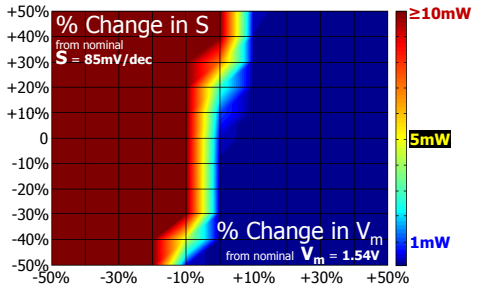

Fig. 9 Write power as a function of voltage margin V_m and AD slope S.

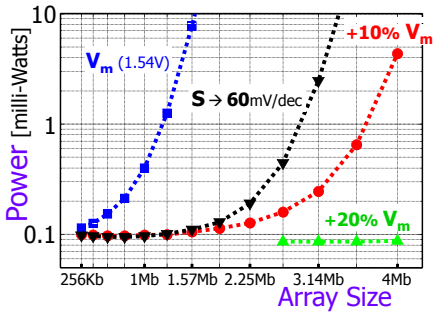

Fig. 10 Any improvement in AD parameters permits significantly larger size arrays.

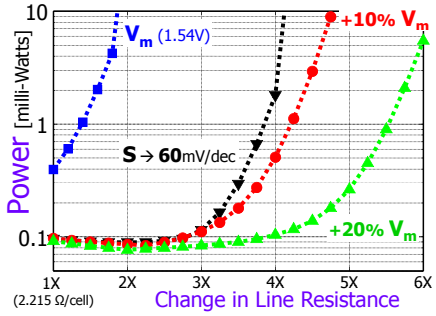

Fig. 11 Alternatively, improved AD parameters can be used to accommodate the higher line resistances of scaled technology nodes.

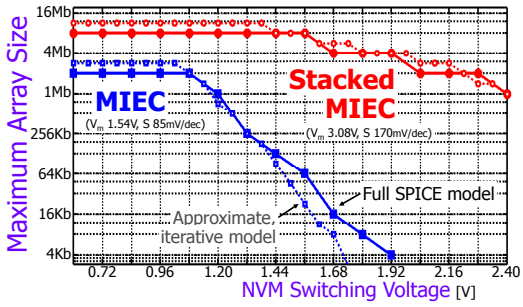

Fig. 12 Maximum achievable array size vs. V_{NVM}. For two stacked MIEC ADs, V_m improvement outweighs degradation in turn-on slope and series resistance. A simple model, iterating out from the selected device, is close to SPICE in accuracy.

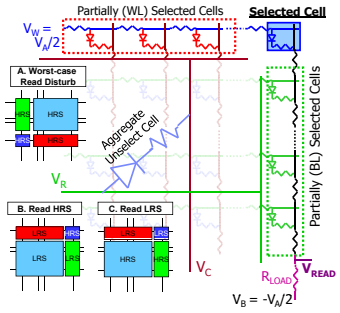

Fig. 13 One aggregate 1AD+1R can model the combined leakage of all unselected crosspoints; read operation adds R_{LOAD} at array periphery. Insets show assumed patterns of stored data.

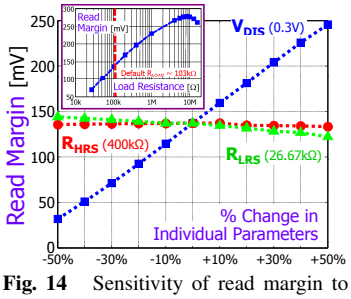

Fig. 14 Sensitivity of read margin to V_{DIS}, R_{HRS} and R_{LRS}. Inset: Read margin is maximized when R_{LOAD} approaches R_{HRS-PF}. Default value of $R_{LOAD} = \sqrt{R_{LRS}R_{HRS}} \sim 103k\Omega$.

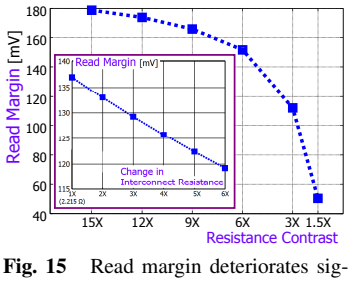

Fig. 15 Read margin deteriorates significantly with loss of resistance contrast (LRS resistance approaches ohmic HRS), and (inset) decreases linearly as interconnect resistance increases.

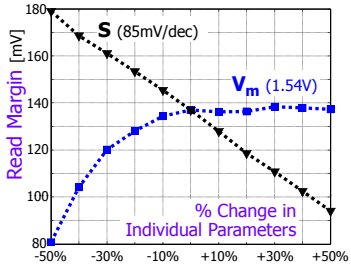

Fig. 16 The impact of V_m and S changes on read margin is significantly less critical than their write power impact (Fig.8).