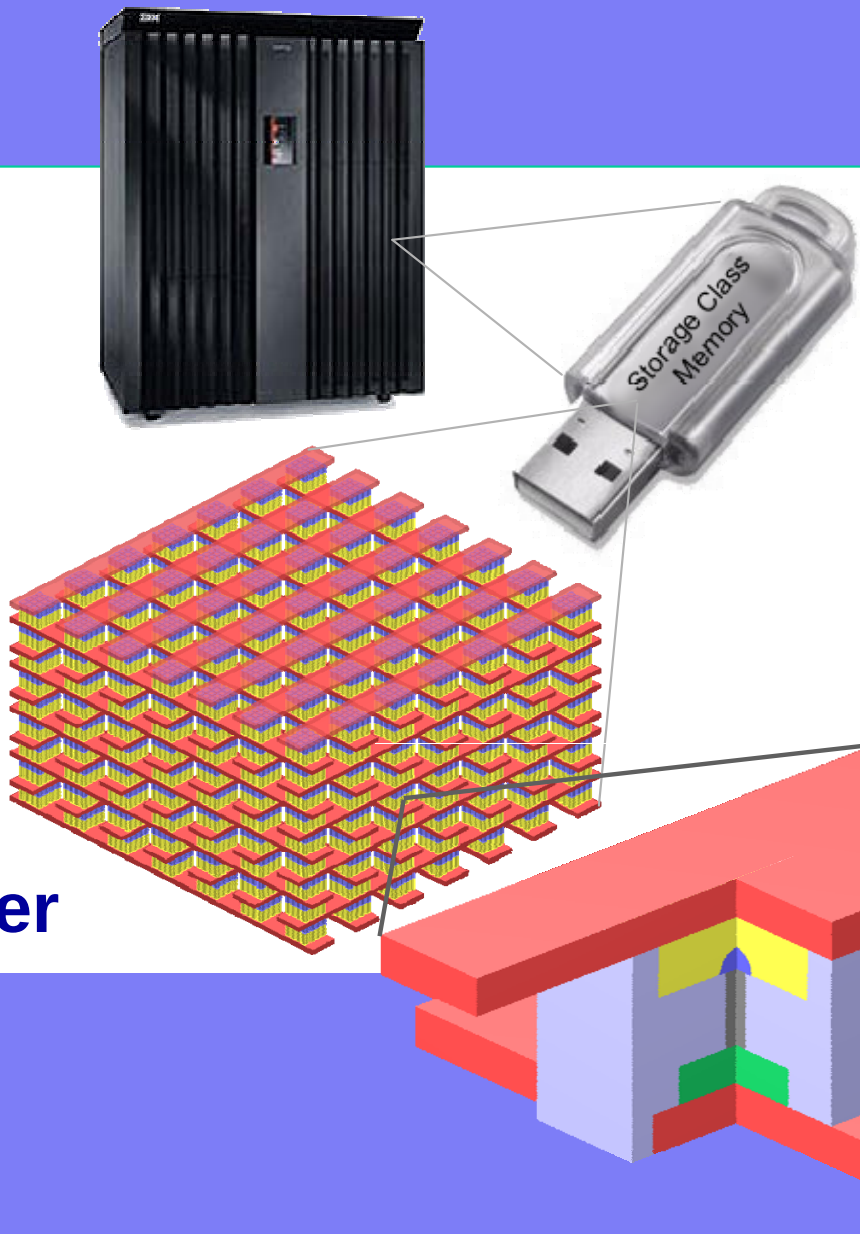
Storage Class Memory

Towards a disruptively low-cost solid-state non-volatile memory



Science & Technology

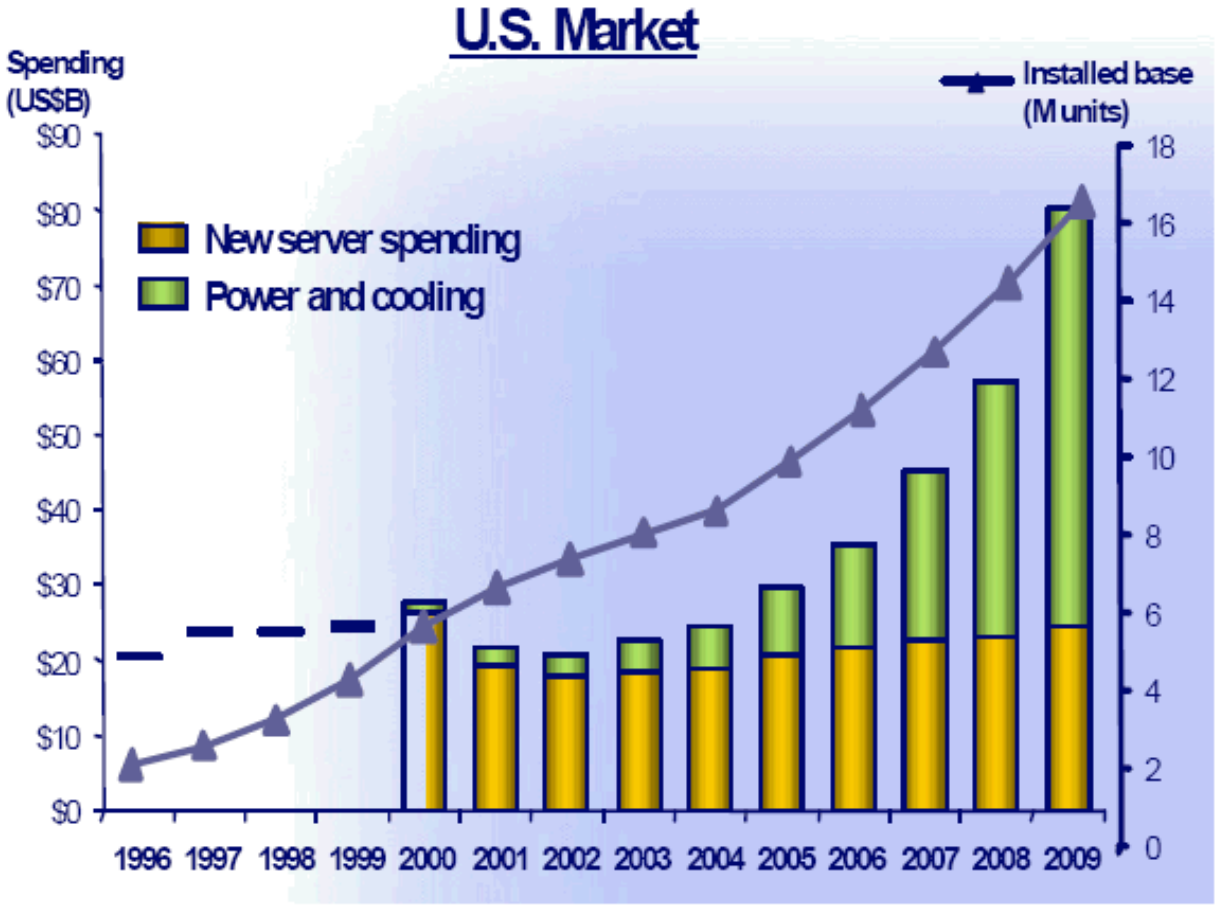
IBM **Almaden Research Center**

January 2013

Power & space in the server room

The cache/memory/storage hierarchy is rapidly becoming the **bottleneck for large systems**.

We know how to create MIPS & MFLOPS cheaply and in abundance,
but **feeding them with data** has become
the performance-limiting *and* most-expensive part of a system (in **both $ and Watts**).



Source IDC: 2006, Document # 201722, "The Impact Of Power and Cooling On Data Center Infrastructure", John Humphreys, Jed Scaramella

Extrapolation to 2020

(at 70% CGR → need **2 GIOP/sec**)

- **5 million HDD**
  - **16,500** sq. ft. !!
  - **22 Mega**watts

R. Freitas and W. Wilcke, *Storage Class Memory: the next storage system technology* –"Storage Technologies & Systems" special issue of the IBM Journal of R&D (2008)

...yet critical applications are also undergoing a paradigm shift

	Compute-centric paradigm	**Data-centric paradigm**
Main Focus:	**Solve differential equations**	**Analyze petabytes of data**
Bottleneck:	***CPU / Memory***	***Storage & I/O***
Typical Examples:	Computational Fluid Dynamics Finite Element Analysis Multi-body Simulations	Search and Mining Analyses of social/terrorist networks Sensor network processing Digital media creation/transmission Environmental & economic modeling

Extrapolation to 2020

(at 90% CGR → need **1.7 PB/sec**)

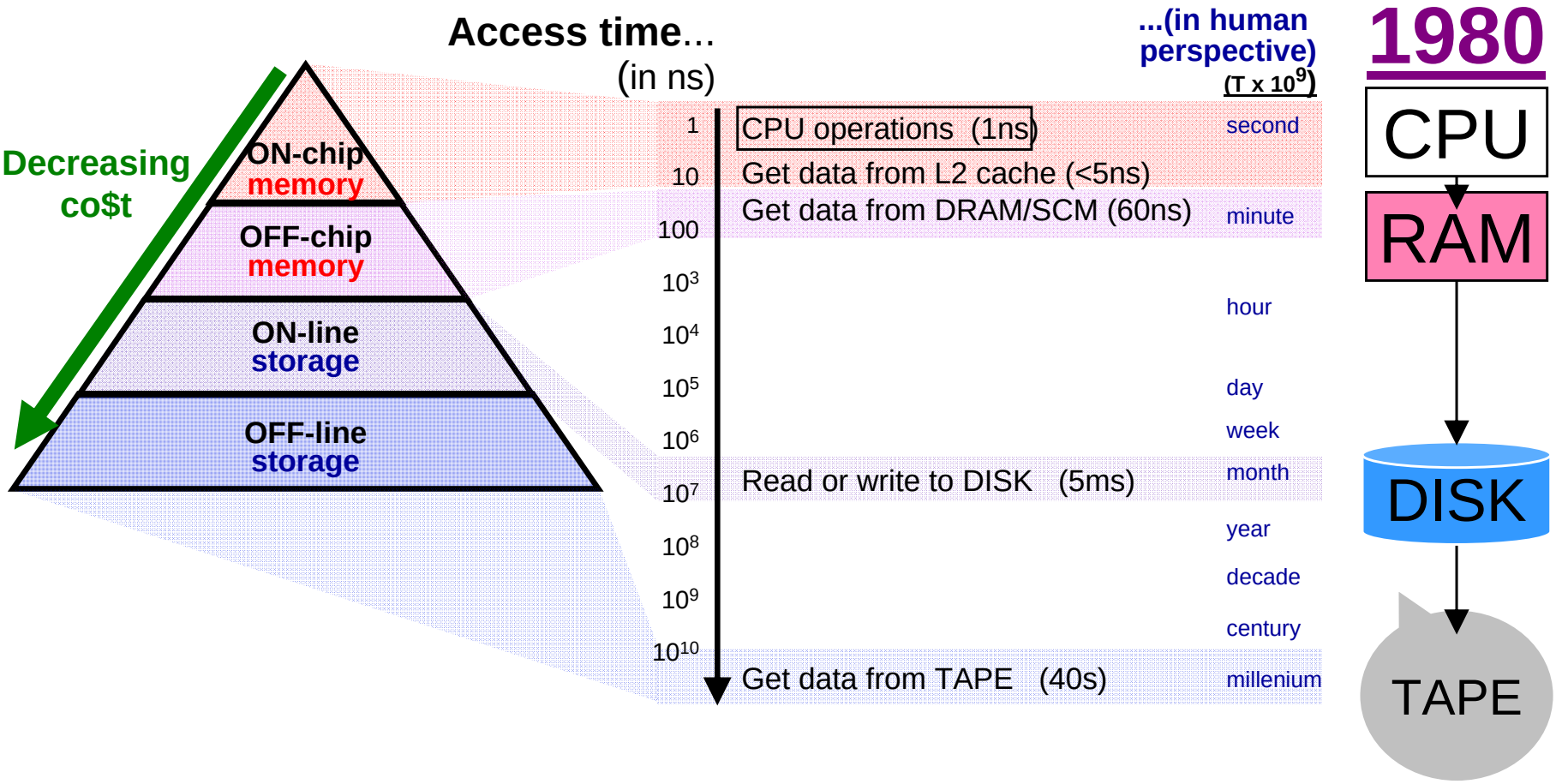
- **5.6 million HDD**
  - **19,000** sq. ft. !!
  - **25 Megawatts**

(at 90% CGR → need **8.4G SIO/sec**)

- **21 million HDD**
  - **70,000** sq. ft. !!
  - **93 Megawatts**

[Freitas:2008]

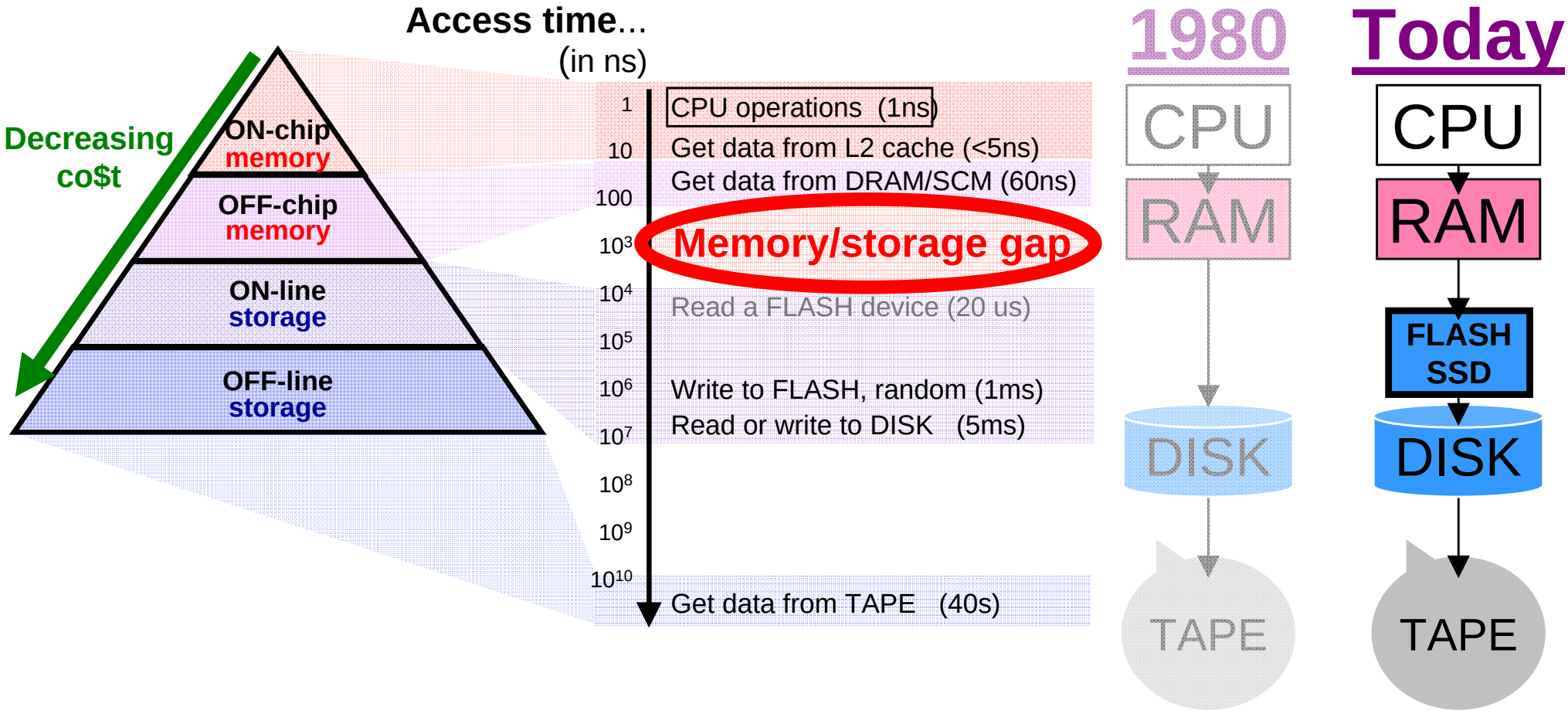
Problem (& opportunity): The access-time gap between memory & storage



- Modern computer systems have long had to be designed around **hiding the access gap** between **memory** and **storage** → caching, threads, predictive branching, etc.

- "Human perspective" – if a CPU instruction is analogous to a 1-second decision by a human, retrieval of data from off-line tape represents an analogous delay of 1250 years

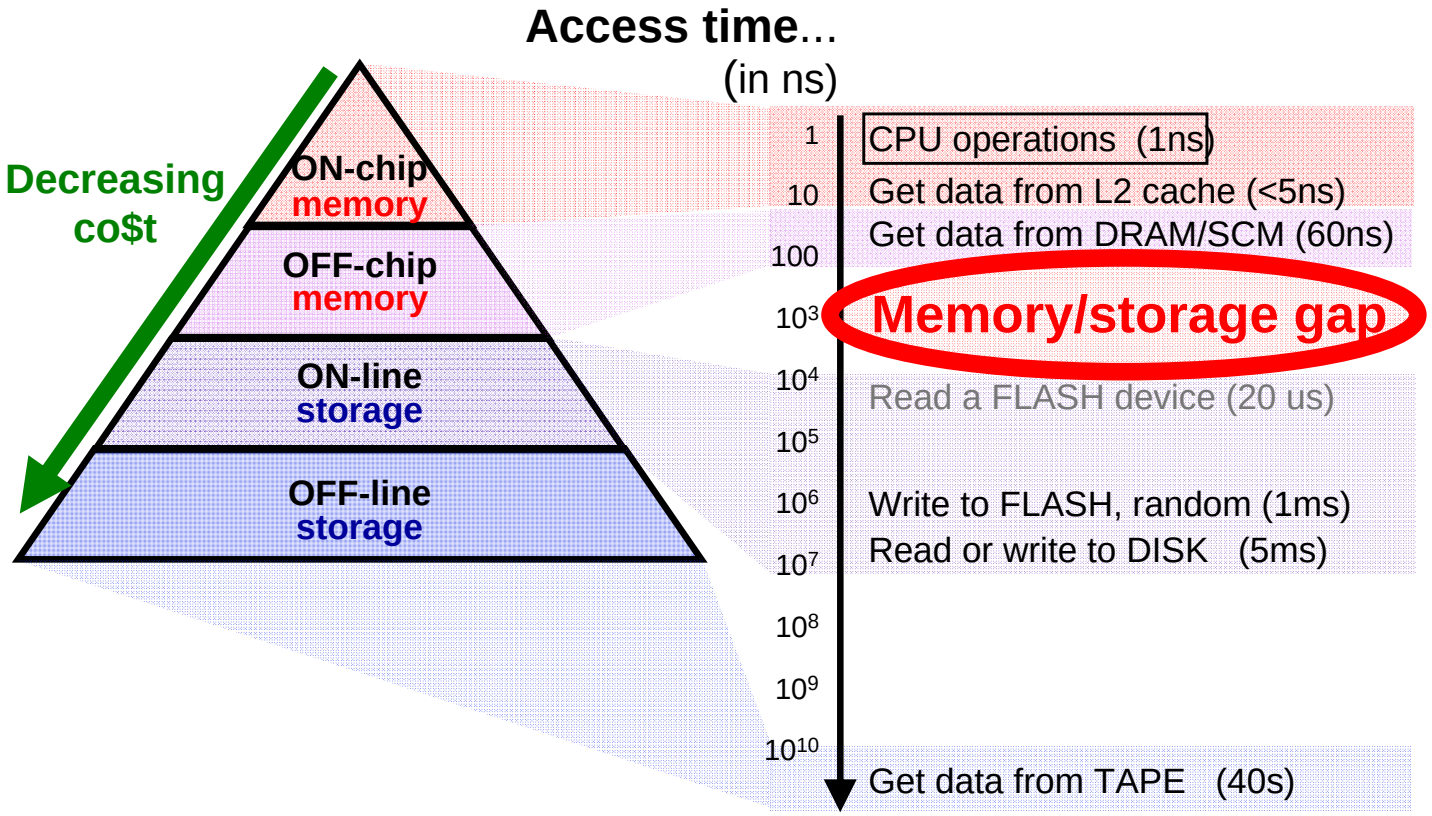
Problem (& opportunity): The access-time gap between memory & storage



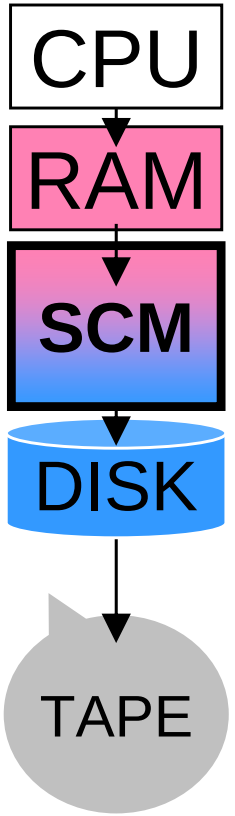
- Today, **Solid-State Disks** based on NAND Flash can offer fast ON-line storage, and storage capacities are increasing as devices scale down to smaller dimensions...

  ...but while prices are dropping, the **performance gap** between memory and storage remains significant, and the already-**poor device endurance** of Flash is getting worse.

Problem (& opportunity): The access-time gap between memory & storage



Near-future



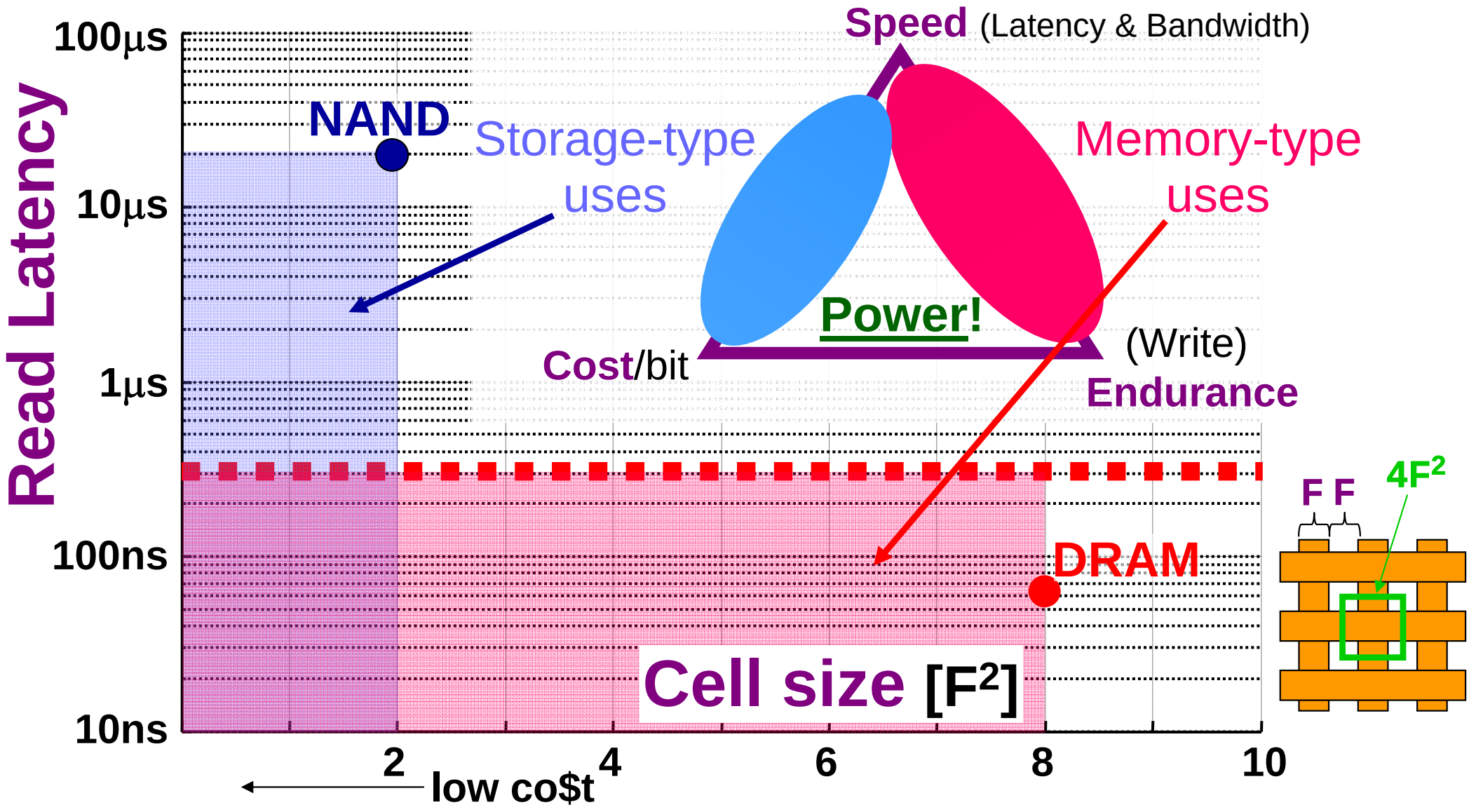
Research into new solid-state non-volatile memory candidates
– originally motivated by finding a "successor" for NAND Flash –
has opened up several interesting ways to change the memory/storage hierarchy...

1) **Embedded** Non-Volatile Memory – low-density, fast ON-chip NVM
2) **Embedded** Storage – low density, slower ON-chip storage

3) M-type **Storage Class Memory** – **high-density**, fast OFF- (or ON*)-chip NVM
4) S-type **Storage Class Memory** – **high-density**, very-near-ON-line storage

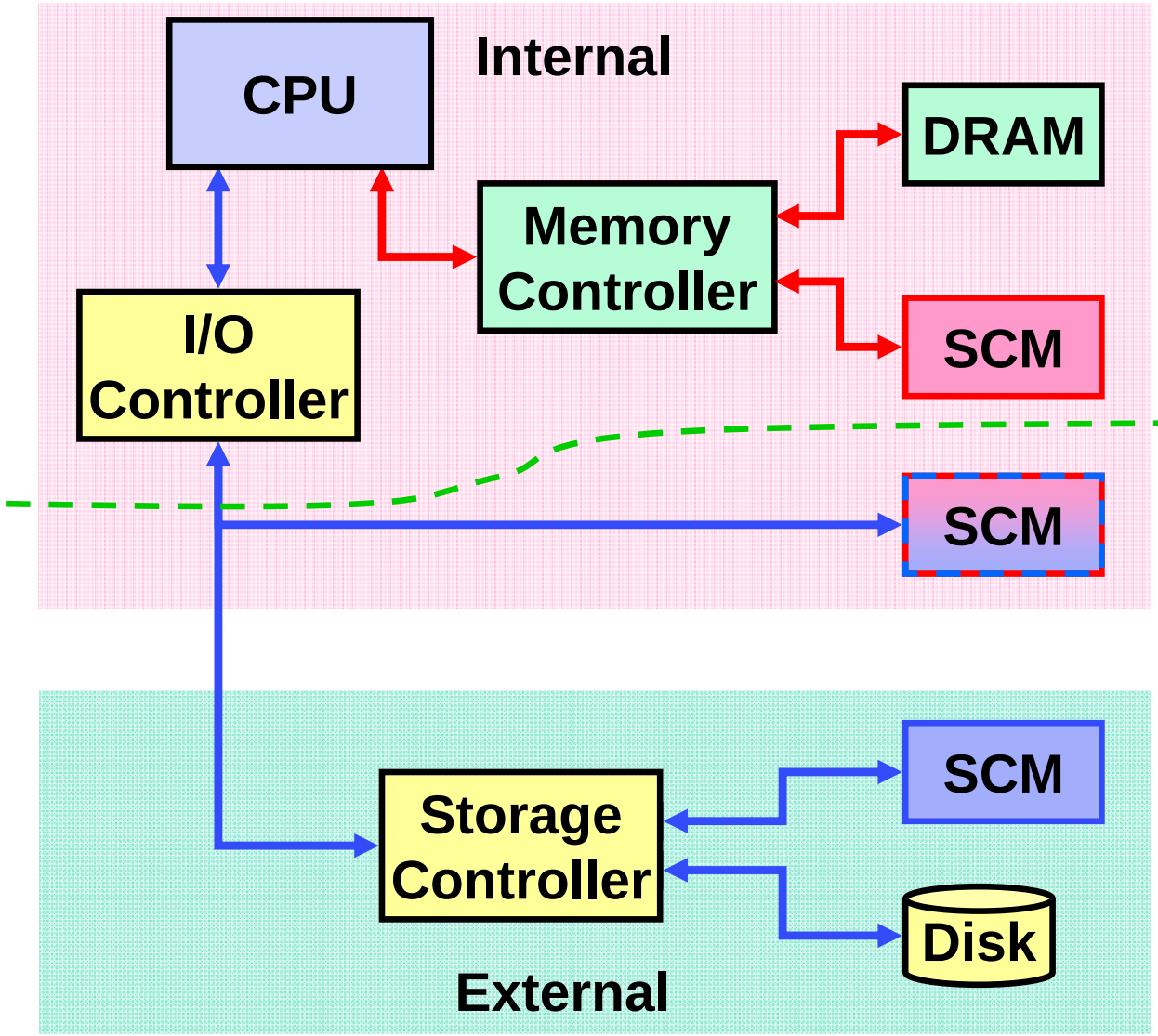
* ON-chip using 3-D packaging

Storage-type vs. memory-type Storage Class Memory



The cost basis of semiconductor processing is well understood – the paths to higher density are
1) shrinking the minimum lithographic pitch **F**, and 2) storing **more bits PER 4F²**

S-type vs. M-type SCM



M-type: Synchronous

- Hardware managed
- Low overhead
- Processor waits
- New NVM → **not Flash**
- Cached or pooled memory
- Persistence (data survives despite component failure or loss of power) requires redundancy in system architecture

S-type: Asynchronous

- Software managed
- High overhead
- Processor doesn't wait, (process-, thread-switching)
- Flash or new NVM
- Paging or storage
- Persistence → RAID

Competitive Outlook among emerging NVMs

Future NAND applications
(consumer devices, etc.)

- **3-D NAND** (but crossover to succeed 20nm conventional NAND may require >50 layers!)
- **PCM? / RRAM?**

Future NOR applications
(program code, etc.)

- **PCM** (but market disappearing)

Embedded Storage
(low density, slower ON-chip storage)

- **NAND?** (but complicated process)
- **RRAM? / PCM?**

S-type **Storage Class Memory**
(**high-density**, very-near-ON-line storage)

1) **PCM? / RRAM?**
2) **Racetrack?** (future?)

M-type **Storage Class Memory**
(**high-density**, fast OFF- (or ON*)-chip NVM)

- **CBRAM? STT-RAM?**
- **PCM? / RRAM?**
- **Racetrack?** (future?)

Embedded Non-Volatile Memory
(low-density, fast ON-chip NVM)

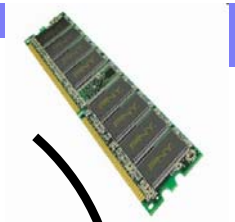
- **STT-RAM? CBRAM?**

High Speed

Low co$t

* ON-chip using 3-D packaging

Paths towards SCM



Device Availability

Co$t

Capital investment

Applications

NAND — **3-D NAND** → **Future NAND applications** (consumer devices, etc.)

unlikely, but possible path

1-10us emerging **NVM**

RRAM? PCM? CBRAM?

→ **Embedded** Storage (low density, slower ON-chip storage) → S-type **SCM** (**high-density**, near-ON-line storage)

≪1us emerging **NVM**

STT-RAM? CBRAM? PCM?? / RRAM??

→ **Embedded** Non-Volatile Memory (low-density, fast ON-chip NVM) → M-type **SCM** (**high-density**, fast OFF-(or ON*) -chip NVM)

* ON-chip using 3-D packaging

DRAM → **Future DRAM** (working memory, etc.)

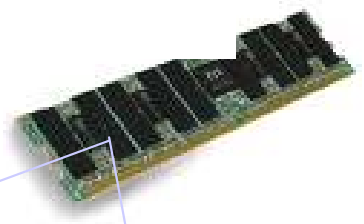
NVM candidates for SCM

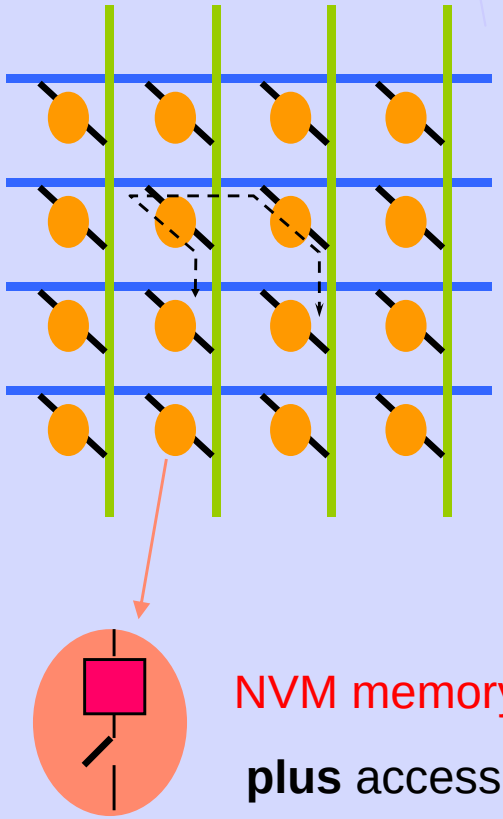
1) **NVM element**

- **Improved FLASH**
- **Magnetic Spin Torque Transfer**
  - → **STT-RAM**
  - → **Magnetic Racetrack**
- **Phase Change RAM**
- **Resistive RAM**

2) High-density access device (A.D.)

- **2-D –** silicon transistor or diode
- **3-D → higher density per $4F^2$**
  - polysilicon diode (but <400°C processing?)
  - MIEC A.D. (Mixed Ionic-Electronic Conduction)
  - OTS A.D. (Ovonic Threshold Switch)
  - Conductive oxide tunnel barrier A.D.





NVM memory element

plus access device

Generic SCM Array

Limitations of Flash

Asymmetric performance

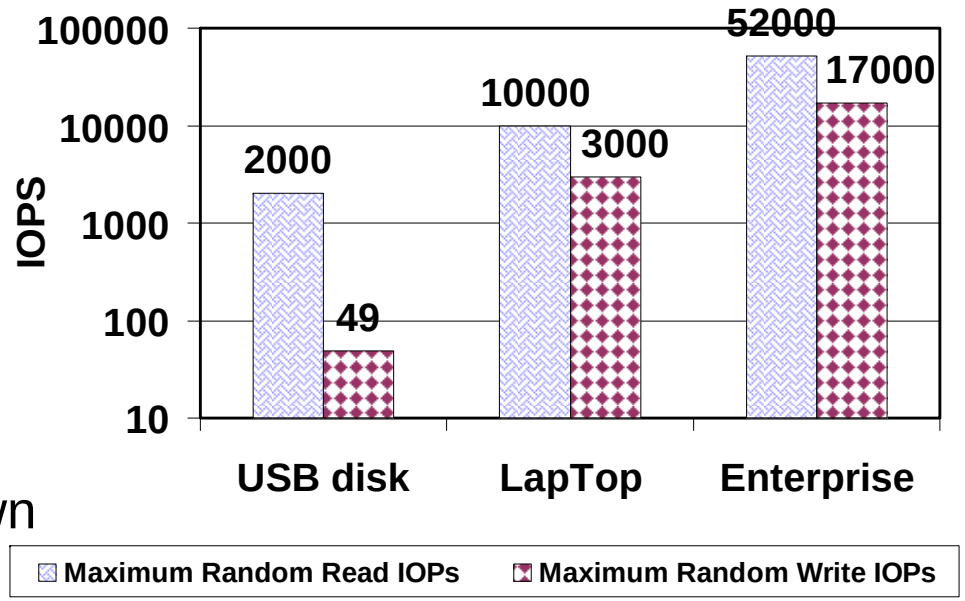
Writes much slower than reads

Program/erase cycle

Block-based, no write-in-place

Data retention and Non-volatility

Retention gets worse as Flash scales down

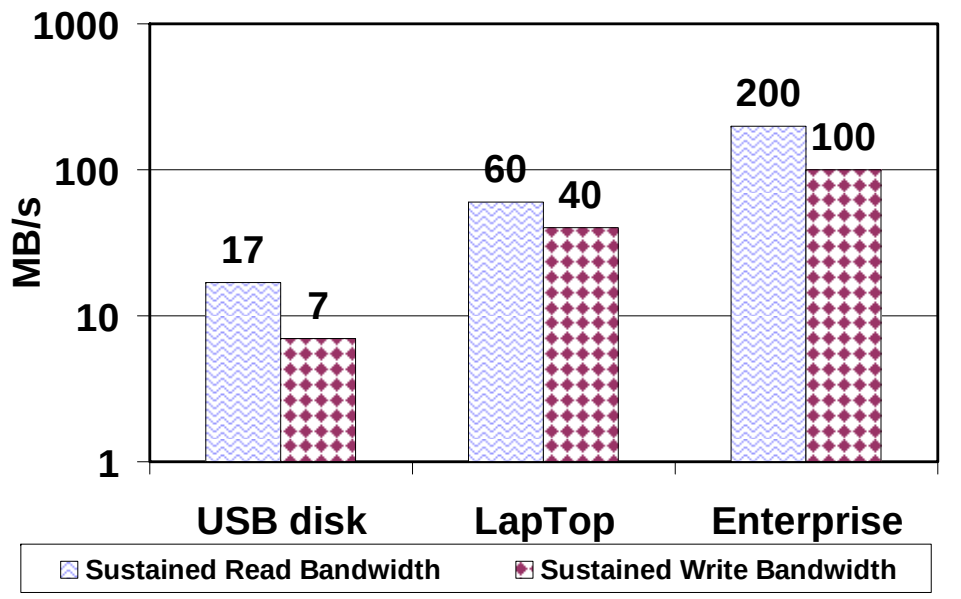


Endurance

- Single level cell (SLC) → 10^5 writes/cell
- Multi level cell (MLC) → 10^4 writes/cell
- Triple level cell (TLC) → ~300 writes/cell

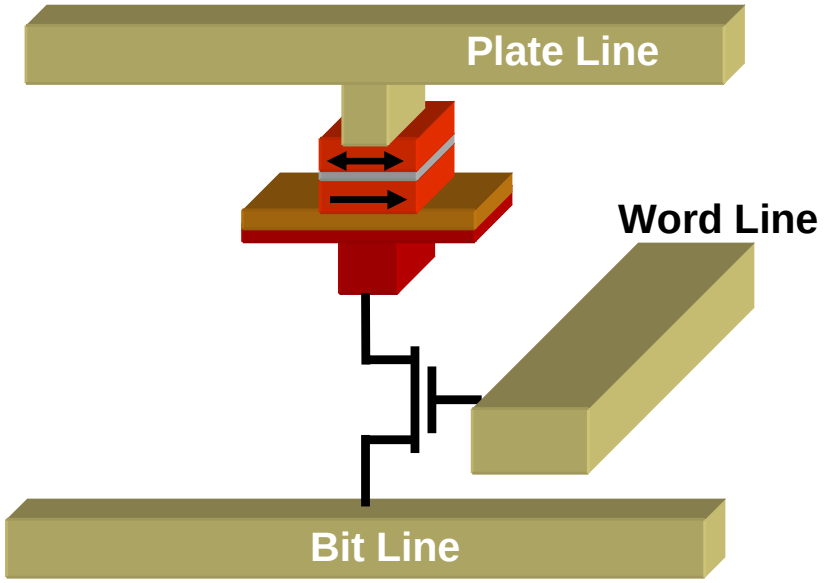
Future outlook

- Scaling focussed solely on density
- 3-D schemes exist but are complex



STT (Spin-Torque-Transfer) RAM

• Controlled switching of free magnetic layer in a magnetic tunnel junction using current, leading to two distinct resistance states



Strengths

- Inherently very fast → **almost as fast as DRAM**
- **Much better endurance** than Flash or PCM
- Radiation-tolerant
- Materials are Back-End-Of-the-Line compatible
- Simple cell structure → reduced processing costs

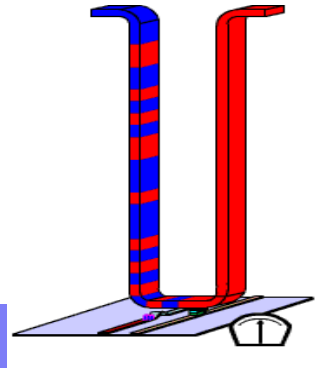
Weaknesses

- Achieving low switching current/power is not easy
- Resistance contrast is quite low (2-3x) → achieving **tight distributions** is ultra-critical
- High-temperature retention **strongly affected by scaling** below F~50nm
- Tradeoff between fastest switching and switching reliability

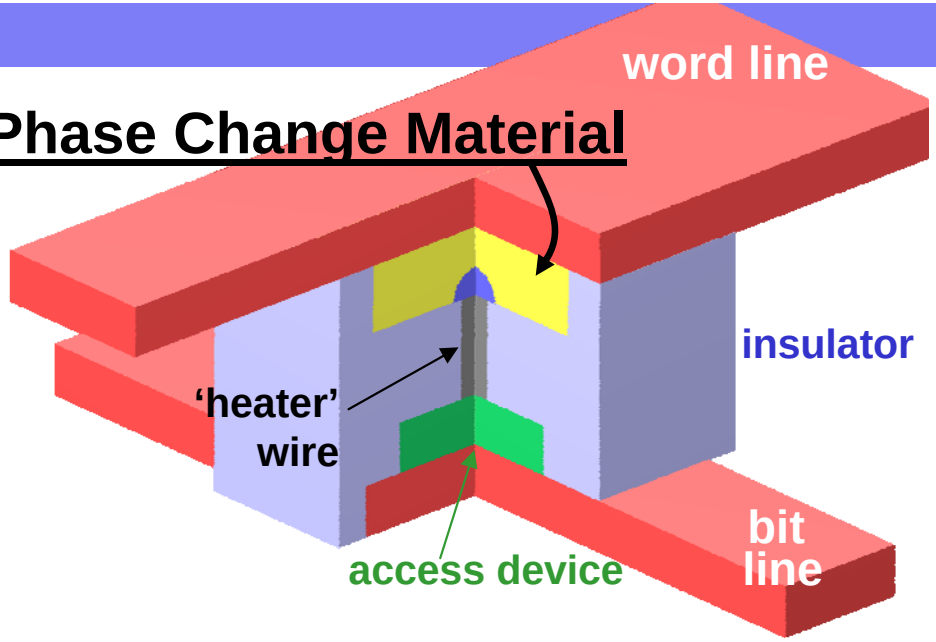
Outlook:

Strong outlook for an Embedded Non-Volatile Memory to replace/augment DRAM.

While near-term prospects for high-density SCM with STT-RAM may seem dim, **Racetrack Memory** offers hope for using STT concepts to create vertical "shift-register" of domain walls → potential densities of 10-100 bits/F^2



Phase-change RAM



- Switching between **low-resistance** crystalline, and **high-resistance** amorphous phases, controlled through power & duration of electrical pulses

Strengths

- **Very mature** (large-scale demos & products)
- Industry consensus on material → GeSbTe or GST
- Large resistance contrast → analog states for **MLC**
- Offers **much better endurance** than Flash
- Shown to be **highly scalable** (still works at ultra-small **F**) and Back-End-Of-the-Line compatible
- Can be very fast (depending on material & doping)

Weaknesses

- RESET step to high resistance requires melting → **power-hungry**, thermal crosstalk?
  To keep switching power down → sub-lithographic feature and high-current Access Device
  To fill small feature → ALD or CVD → difficult now to replace GST with a better material
  Variability in small features broadens resistance distributions
- 10-year **retention at elevated temperatures** can be an issue → recrystallization
- Device characteristics change over time due to elemental segregation → device failure
- **MLC** strongly affected by relaxation of amorphous phase → "resistance drift"

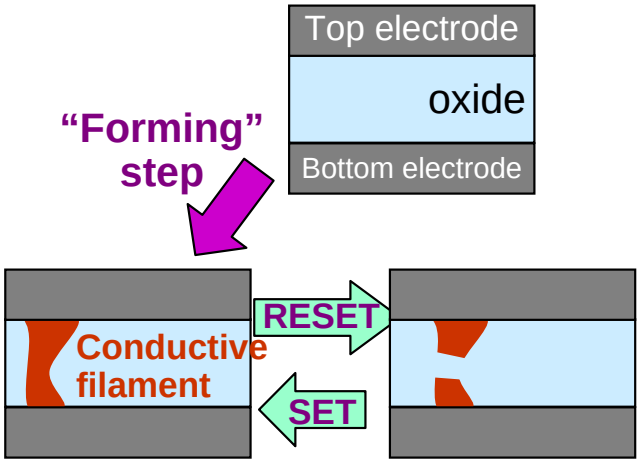
Outlook: NOR-replacement products now shipping → if yield-learning successful and MLC drift-mitigation and/or 3-D Access Devices can offer high-density (=low-cost), then opportunity for NAND replacement, S-type, and then finally M-type SCM may follow

Resistive RAM

Voltage-controlled formation & dissipation of an oxygen-vacancy (or metallic) filament through an otherwise insulating layer

Strengths

- Good retention at elevated-temperatures
- Simple cell structure → reduced processing costs
- Both fast and ultra-low-current switching have been demonstrated
- Some RRAM materials are Back-End-Of-the-Line compatible
- Relatively new field → high hopes for improved material concepts
- Less "gating" Intellectual Property to license
- Some RRAM concepts offer co-integrated NVM & Access Device
- Numerous ongoing development efforts



Weaknesses

- Highly immature technology – wide variation in materials hampers cross-industry learning
- Demonstrated endurance is slightly better than Flash, but lower than PCM or STT-RAM
- **Switching reliability** an issue, even within single devices, and read disturb can be an issue
- An initial high-voltage **"forming"** step is often required
- To attain low RESET switching currents, circuit must constrain current during previous SET
- Unipolar and bipolar versions – bipolar typically better in both write margins & endurance, but then requires an unconventional bipolar-capable Access Device (transistor or diode is out)
- High array yield with minimal "outlier" devices **not yet demonstrated**
- Tradeoff between switching speed, long-term retention, and reliability **not yet explored**

Outlook: Outlook is unclear. Emergence of a strong material candidate offering high array yield & reliability could focus industry efforts considerably. Absent that, many uncertainties remain about prospects for reliable storage & memory products.

NVM candidates for SCM

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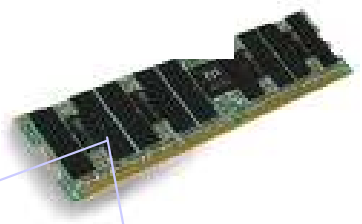
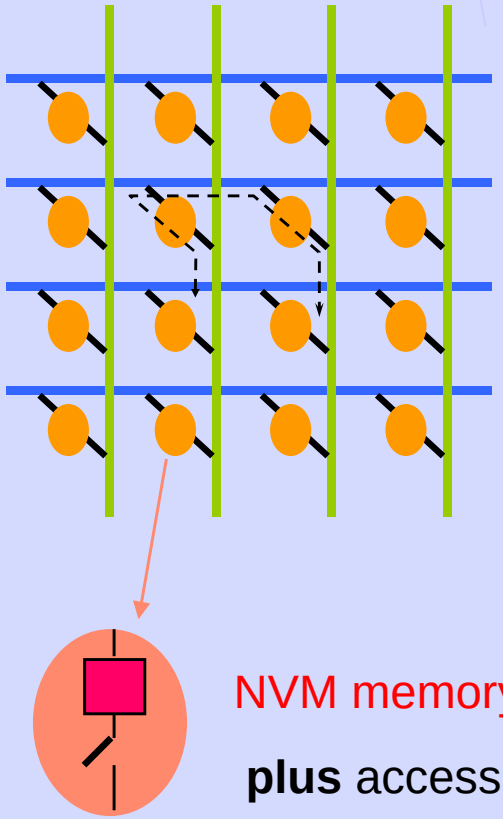




NVM memory element

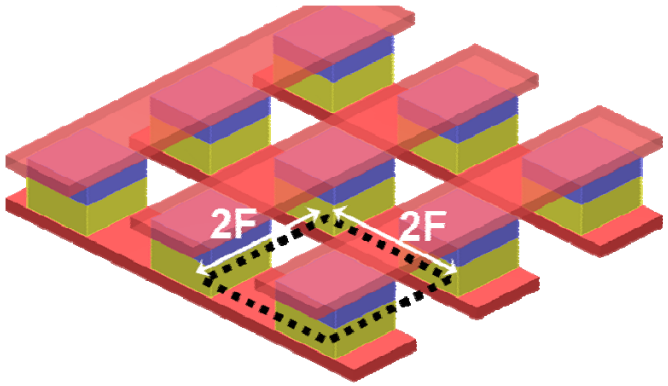
plus access device

Generic SCM Array

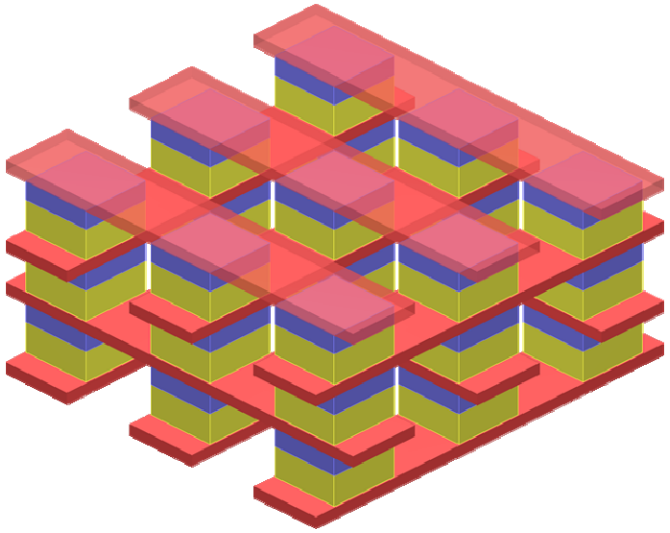
High density → 3D Multilayer Crosspoint Memory Array

As a result of the cost-basis of semiconductor manufacturing, memory cost is inversely related to bit density

(adapted from Burr, EIPBN 2008)



Stack 'L' layers in 3D



Effective cell size: $4F^2$

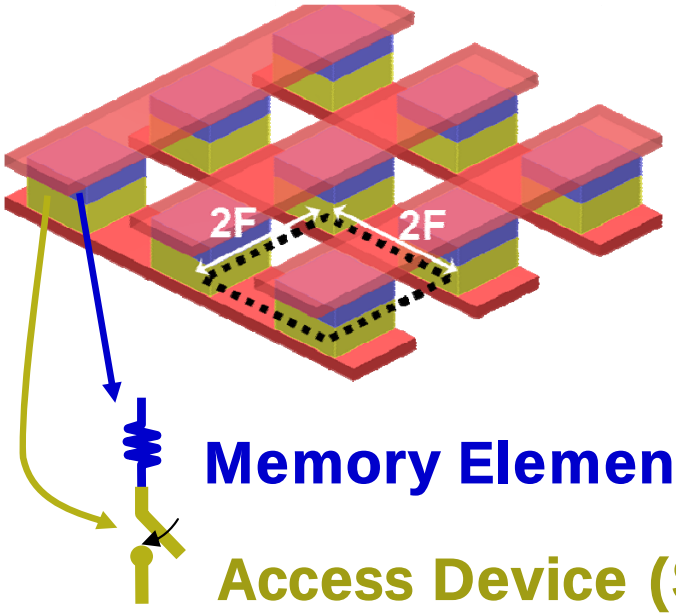
Effective cell size: $4F^2/L$

F = minimum litho. feature size

Since they effectively store more bits per **$4F^2$** footprint,

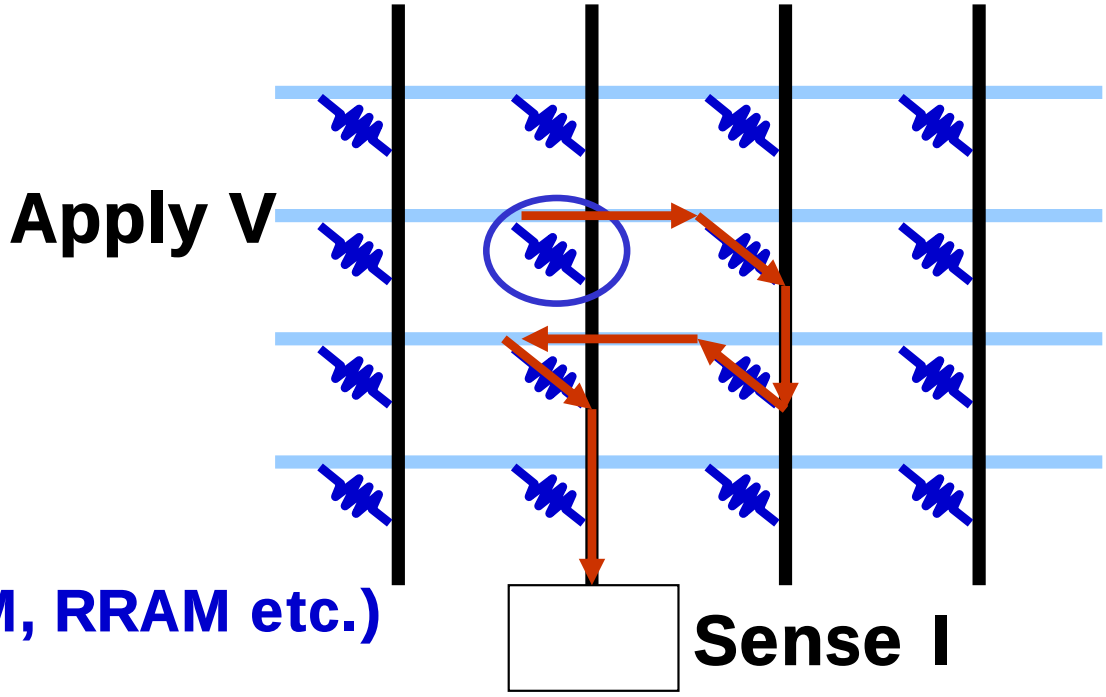
3D crosspoint arrays ⇒ a route to low cost memory

Large arrays require an Access Device at each element



Memory Element (PCM, RRAM etc.)

Access Device (Selector)



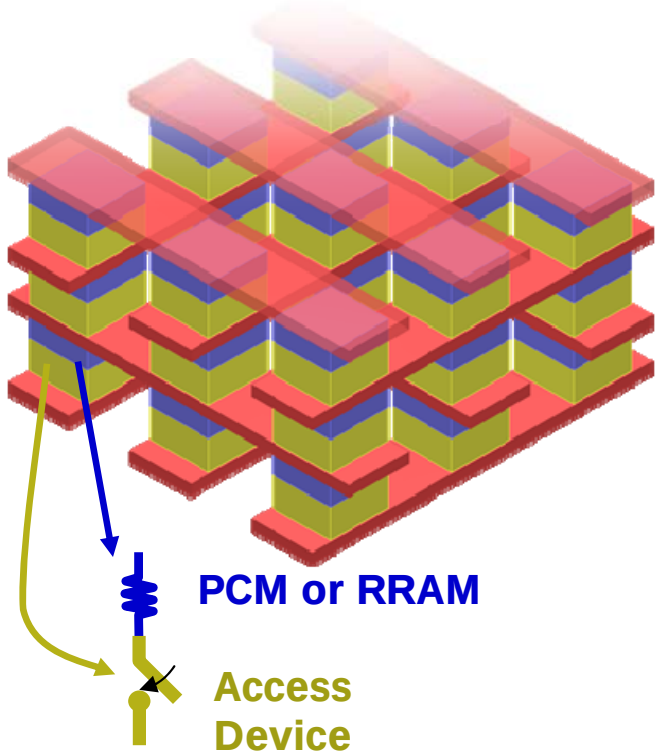
Current 'sneak path' problem

Access device needed in series with memory element

- Cut off current 'sneak paths' that lead to incorrect sensing and wasted power
- Typically diodes used as access devices
- Could also use devices with highly non-linear I-V curves

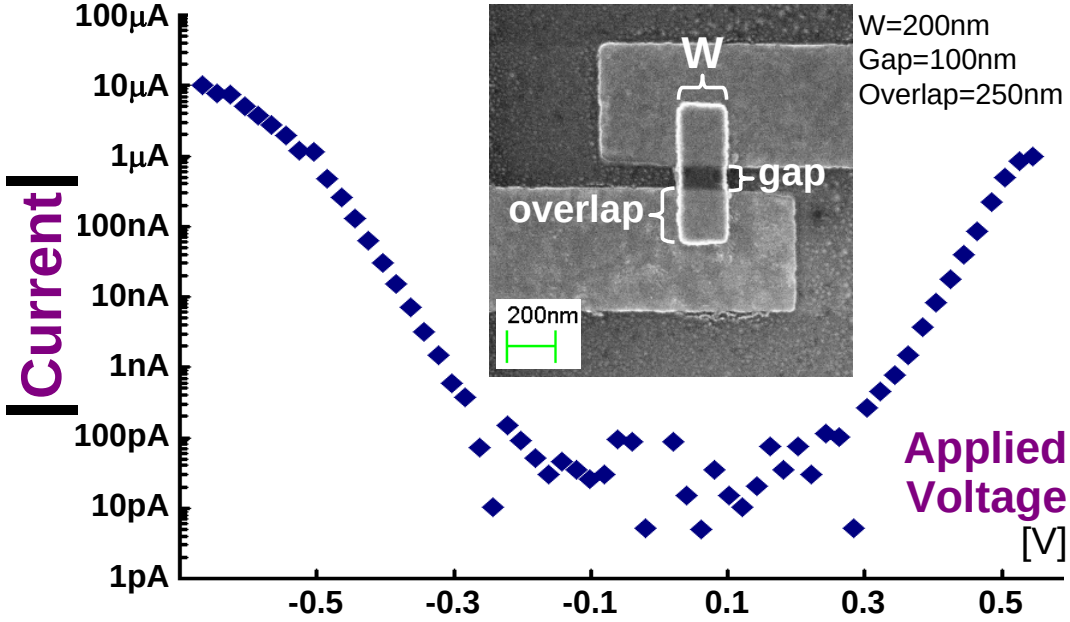
Requirements for an Access Device for 3D Crosspoint Memory

- High ON-state current density
  >10 MA/cm² for PCM / RRAM RESET
- Low OFF-state leakage current
  >10⁷ ON/OFF ratio, and
  wide low-leakage (**< 100pA**) voltage zone to accommodate half-selected cells in large arrays
- Back-End process compatible
  <400C processing to allow 3D stacking
- Bipolar operation
  needed for optimum RRAM operation

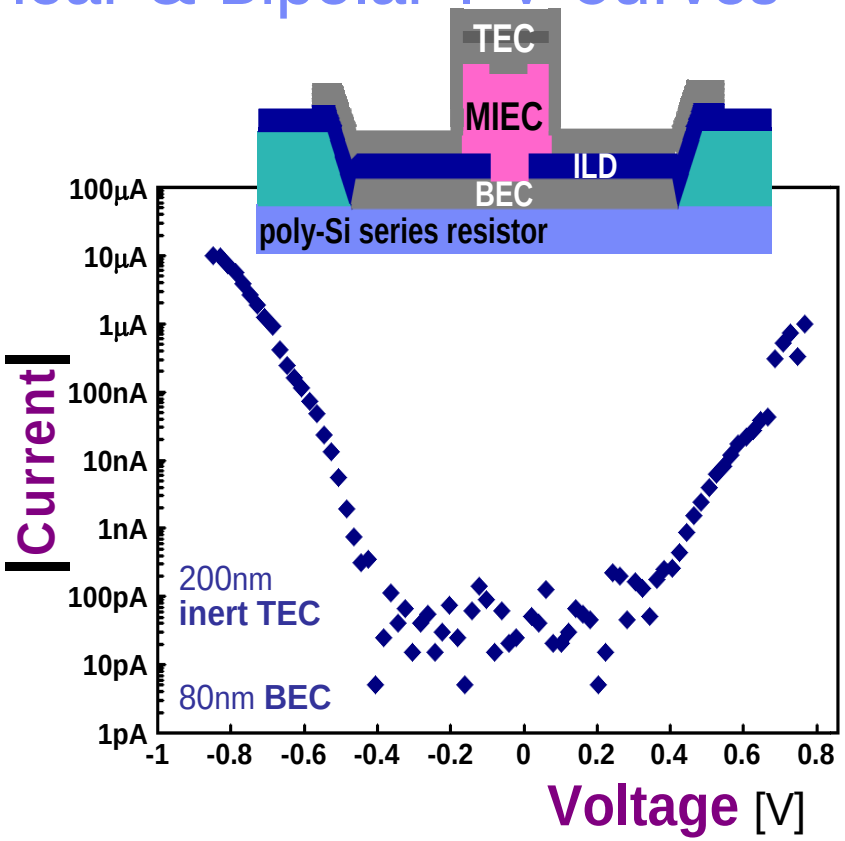


IBM's MIEC-based access device satisfies all these criteria

MIEC access devices offer highly nonlinear & Bipolar I-V Curves



Lateral (bridge) device



Vertical device (scaled TEC)

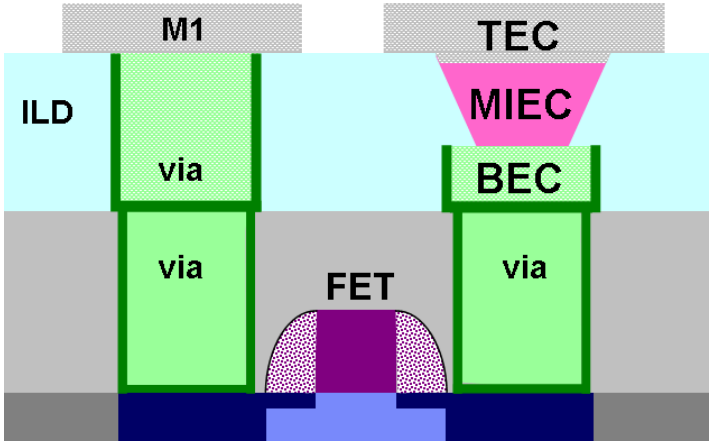
- Devices fabricated on 4inch wafers
- Voltage margin @ 10nA of 0.85V
- Suitable (desirable) for bipolar memory elements such as RRAM

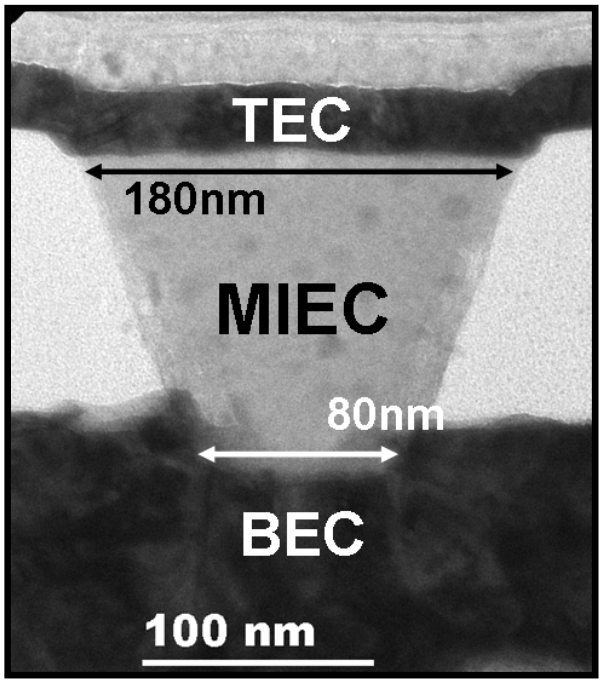
MIEC access devices can operate in both polarities

(Gopalakrishnan *et al*, 2010 VLSI Tech. Sym.)

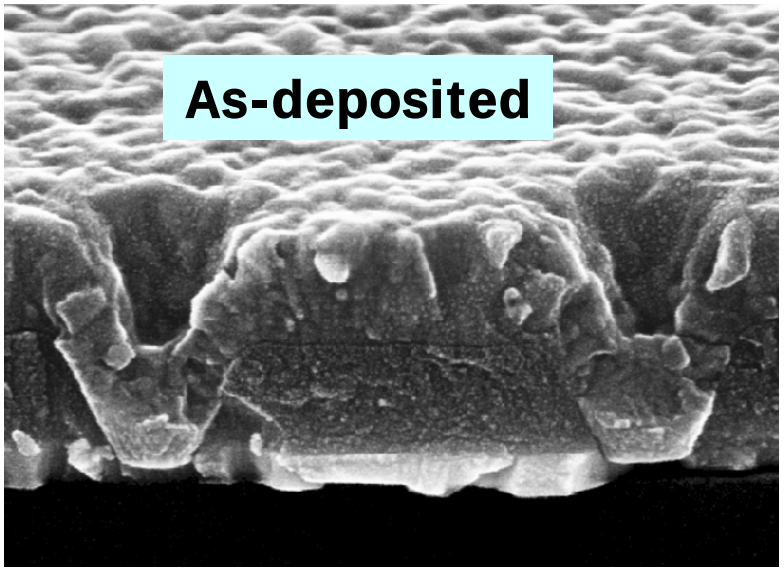
MIEC devices – 200mm wafer integration demonstrated

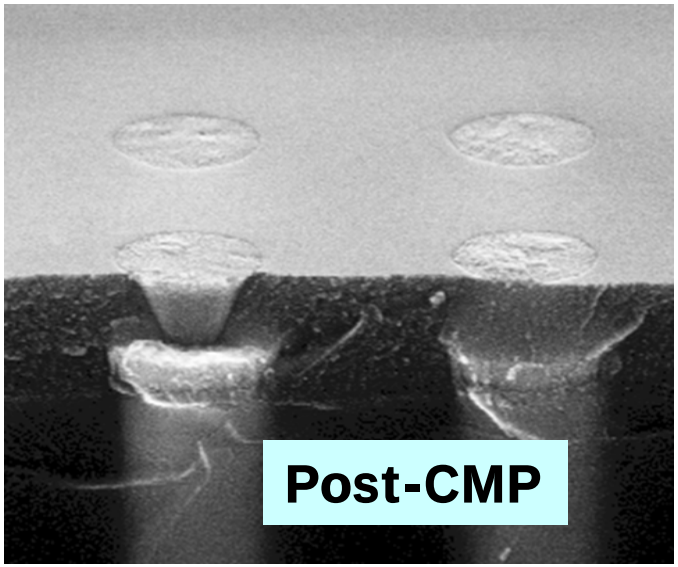
180 nm CMOS Front-End
→ 1T-1MIEC
(1 transistor + 1 MIEC access device)





TEM x-section





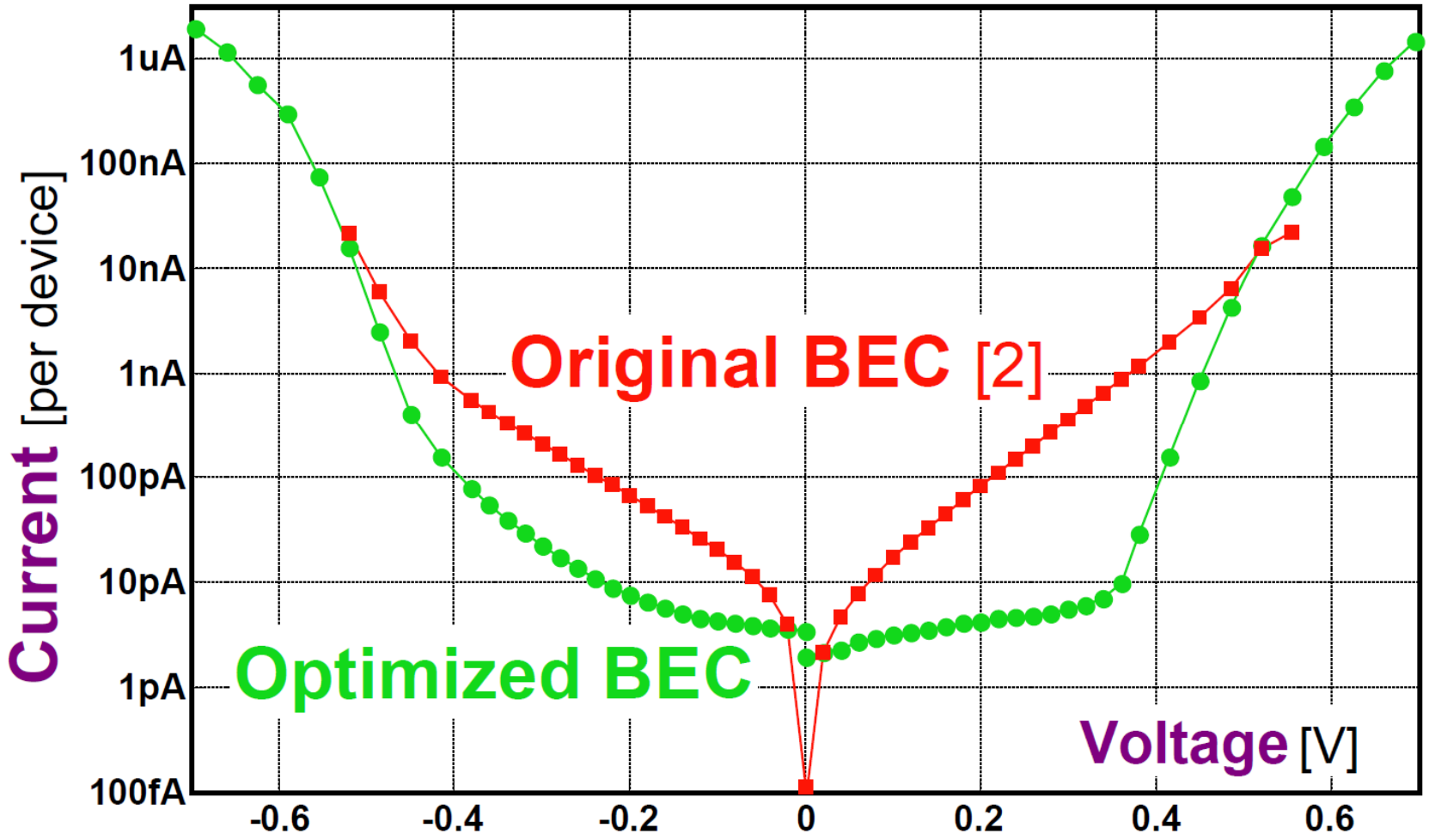
CMP process for MIEC material with modified commercial Cu slurry →

self-aligned MIEC Diode-in-Via (DIV) in a 200 mm wafer process

(Shenoy *et al*, 2011 VLSI Tech. Sym.)

MIEC devices support ultra-low leakage currents

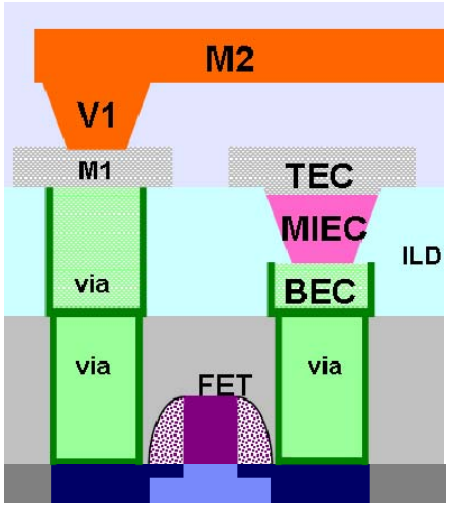
(needed for successful *half-* and *un-select* within large arrays)

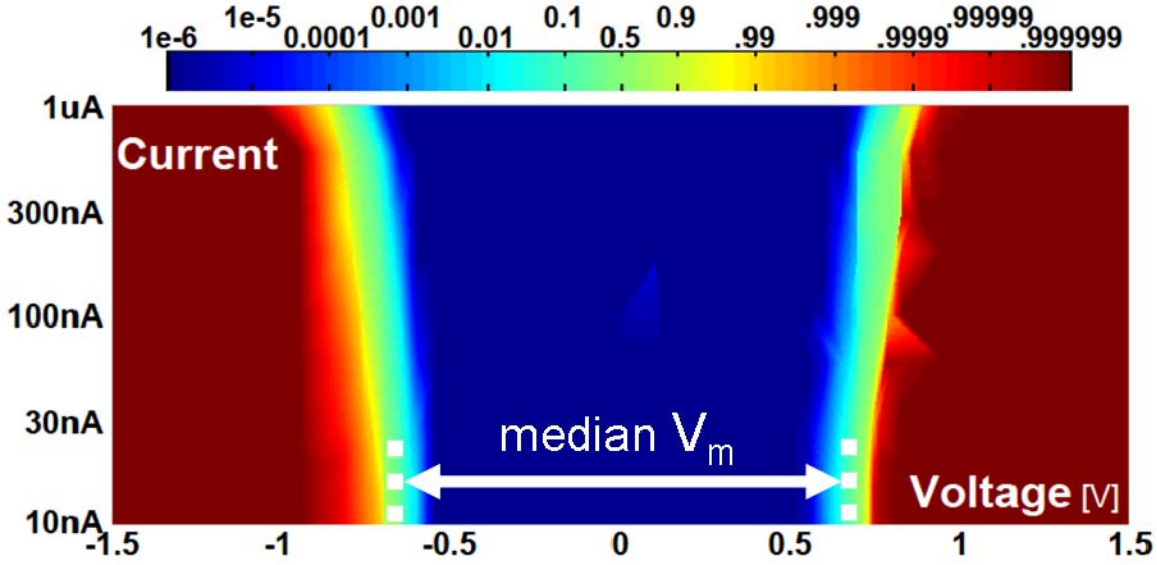


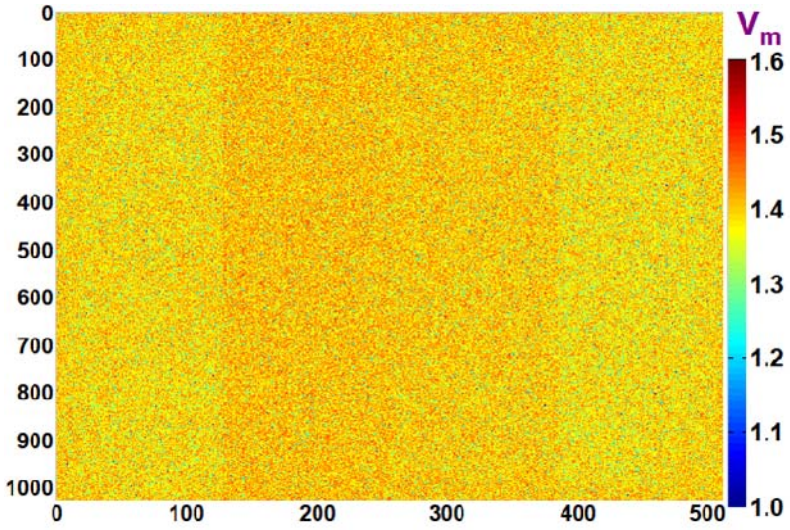
Voltage margin @ 10nA of 1.1V
~10 pA leakage currents near 0V & wide range with <100pA

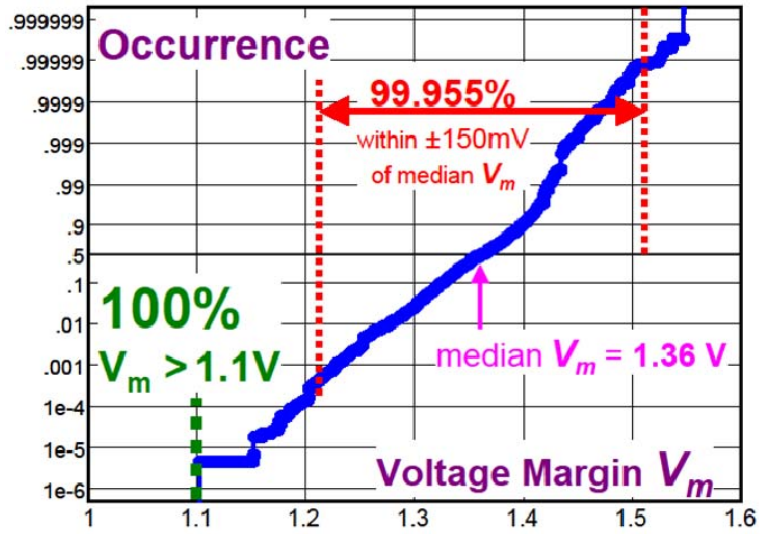
(Burr *et al*, 2012 VLSI Tech. Sym.) (Shenoy *et al*, 2011 VLSI Tech. Sym.)

Large Arrays of MIEC have been integrated at 100% yield







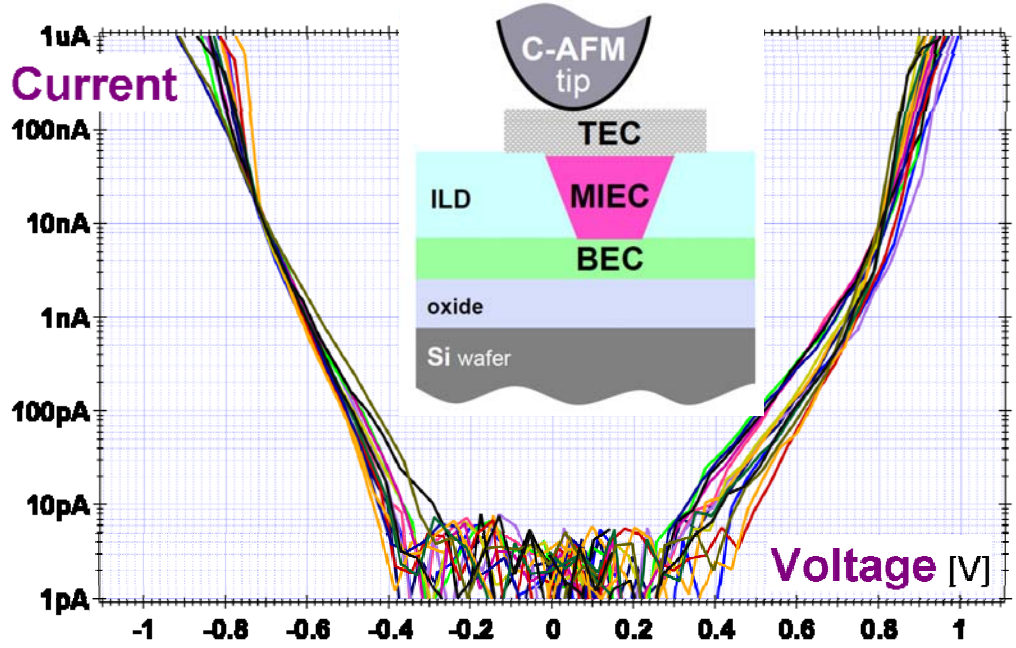


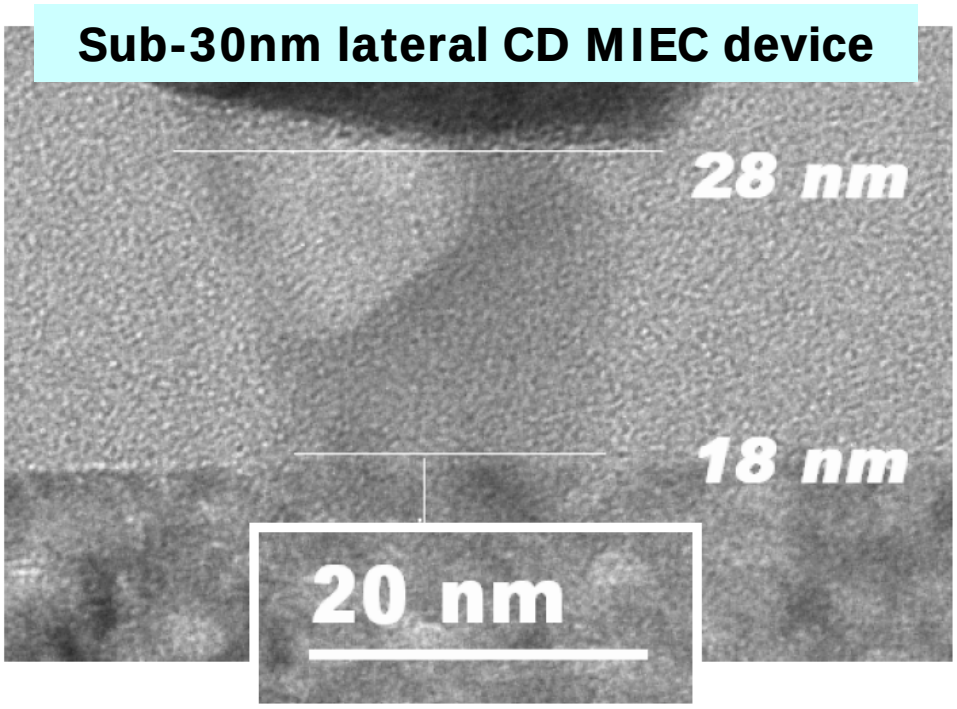
100% yield and tight distributions in 512 kbit 1T-1MIEC array

(Burr *et al*, 2012 VLSI Tech. Sym.)

MIEC access devices are both fast and highly scalable

- High-current switching (RESET) of PCM demonstrated with 15ns pulses
- Low-current reads performed at << 1usec
- Devices retain low leakage characteristics down to <12nm thickness
- **No lower limit to lateral CD scaling has been identified so far**





(Virwani *et al*, 2012 IEDM)

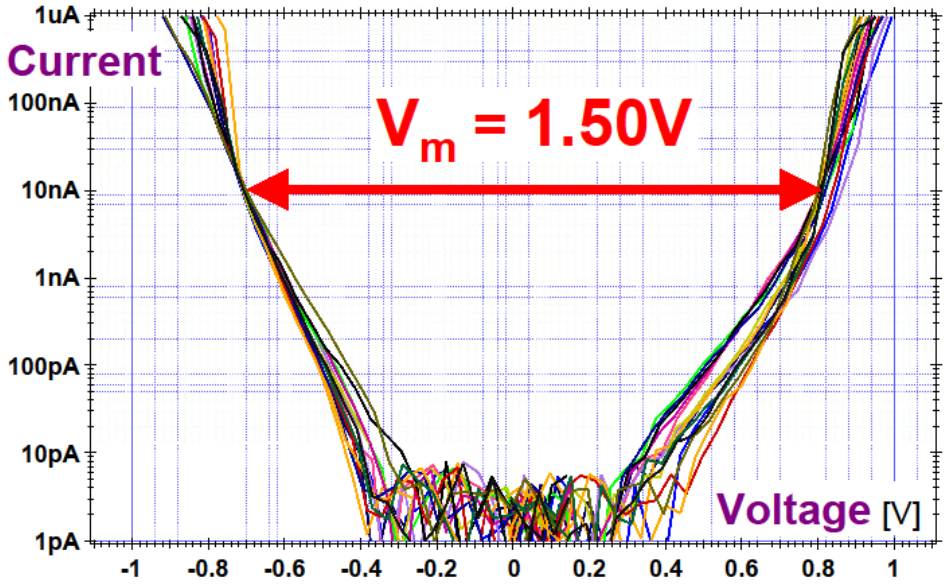
Novel Mixed-Ionic-Electronic-Conduction (MIEC) Access Device

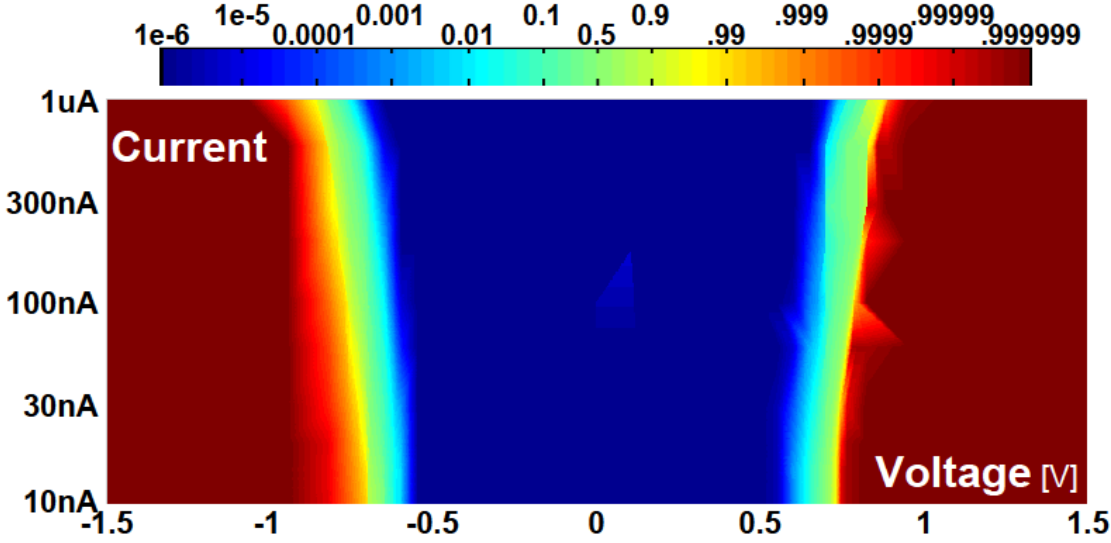
Strengths

- **High** enough **ON currents** for PCM – cycling of PCM has been demonstrated
- **Low** enough **OFF current** for large arrays
- Very large (>>1e10) endurance for typical 5uA read currents
- Voltage margins > 1.5V with tight distributions → sufficient for large arrays
- CMP process demonstrated
- 512kBit arrays demonstrated w/ 100% yield
- Scalable to <30nm CD, <12nm thickness
- Capable of 15ns write, <<1us read

Weaknesses

- Maximum voltage across companion NVM during switching must be low (1-2V) → influences half-select condition and thus achievable array size
- **Endurance during NVM programming** is strongly dependent on programming current





Gopalakrishnan, VLSI 2010
Shenoy, VLSI 2011

Burr, VLSI 2012
Virwani, IEDM 2012

What does the future hold?

- Consumer disk and enterprise tape will persist for the foreseeable future
- Flash will come into its own
- Flash may drive out enterprise disk, and if it doesn't, SCM will
- When will SCM arrive?

  That will depend on the path the NAND industry takes after the 16-20nm node...

  - 3-D NAND succeeds → new NVMs (such as PCM, RRAM, STT-RAM) will develop slowly, driven only by SCM/embedded market
  - 3-D NAND **fails** or is **late** → one new NVM will be driven rapidly by NAND market
- If the latter, SCM could become the dominant storage technology by 2020
- The application software stack will be redesigned to utilize SCM-enabled persistent memory

For more information & *acknowledgements*

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