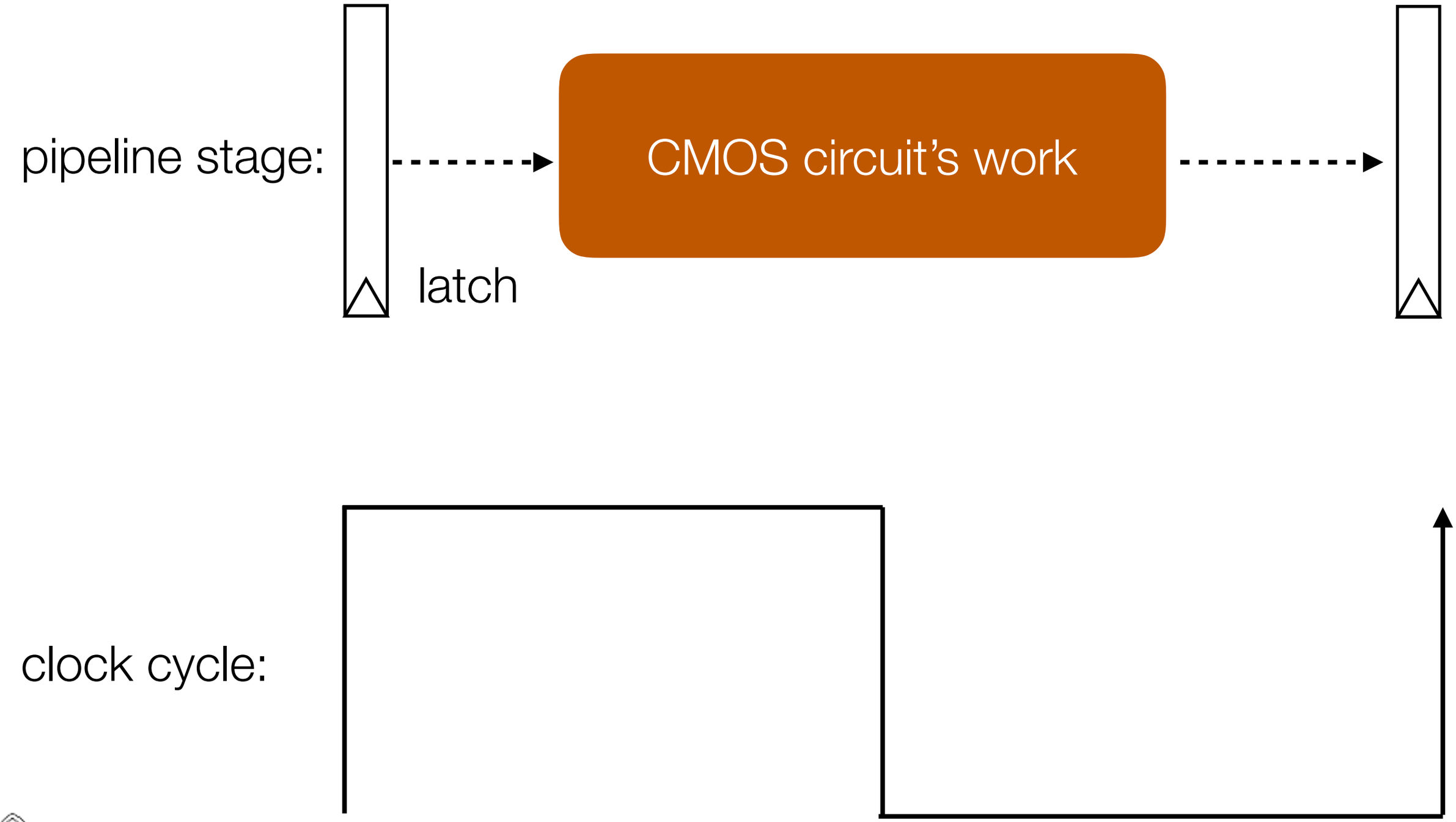
Fine-tuning the Active Timing Margin Control Loop for Maximizing Multicore Efficiency on an IBM POWER Server

Yazhou Zu, Daniel Richins,

Charles R. Lefurgy, Vijay Janapa Reddi

The Pipeline Timing Margin Problem



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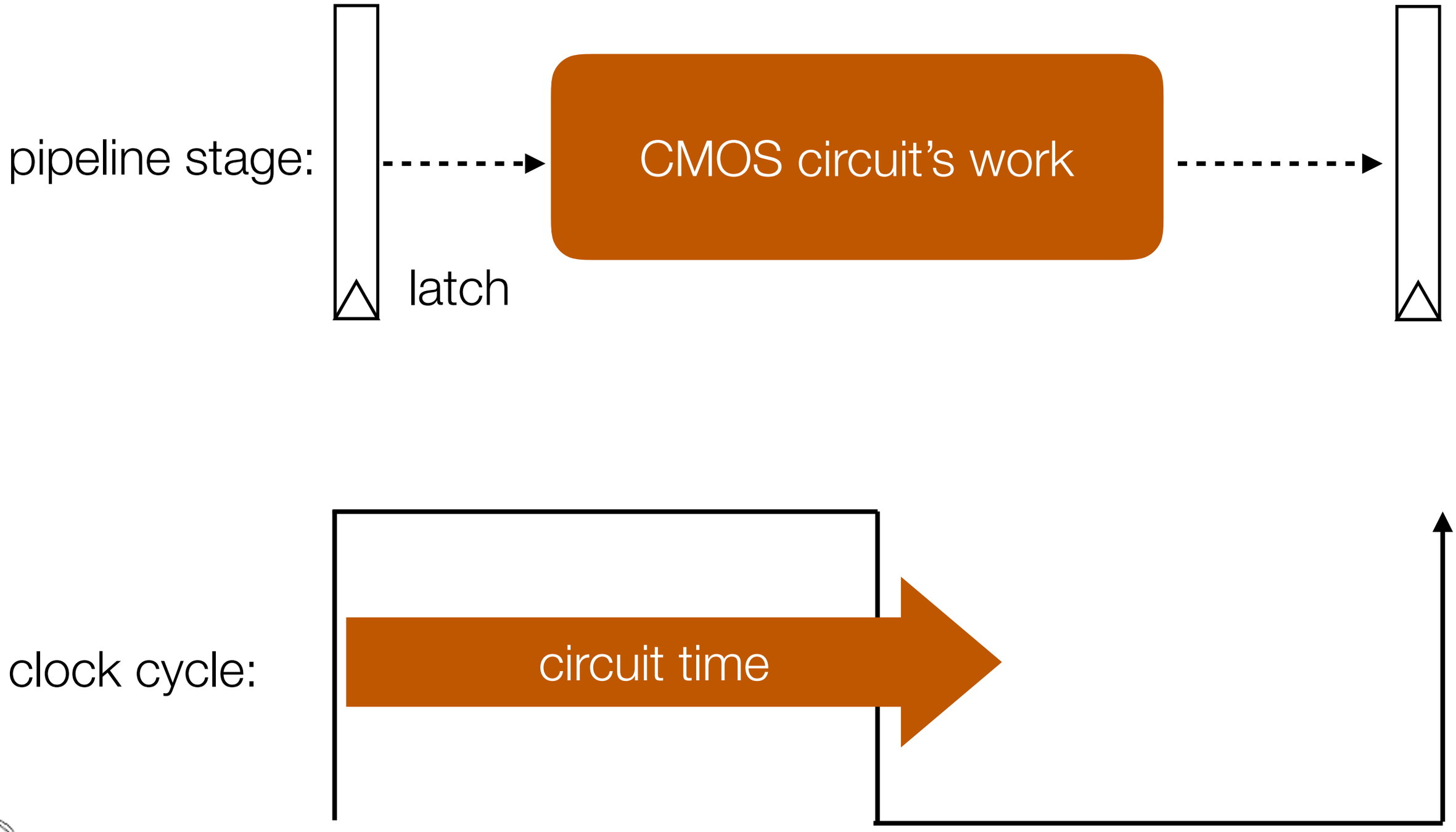

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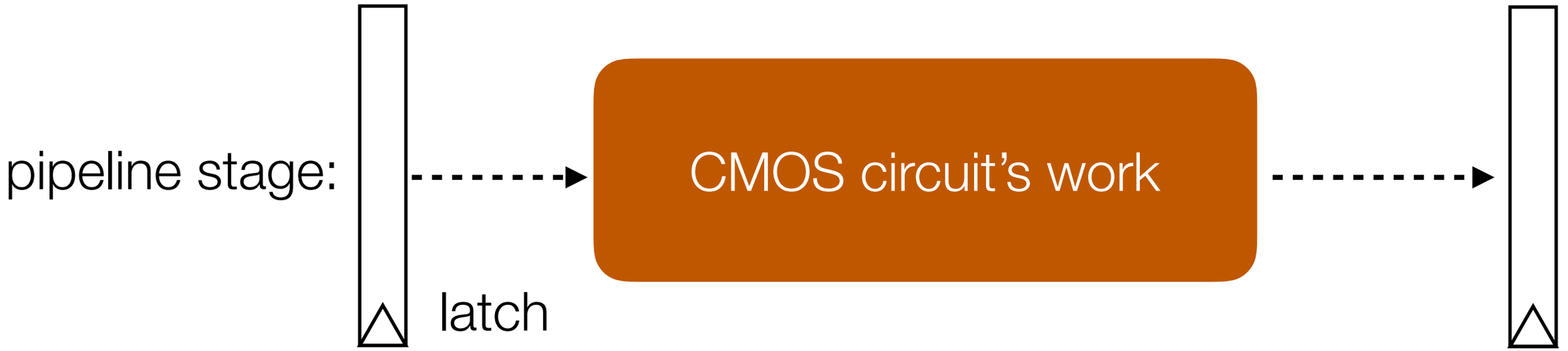

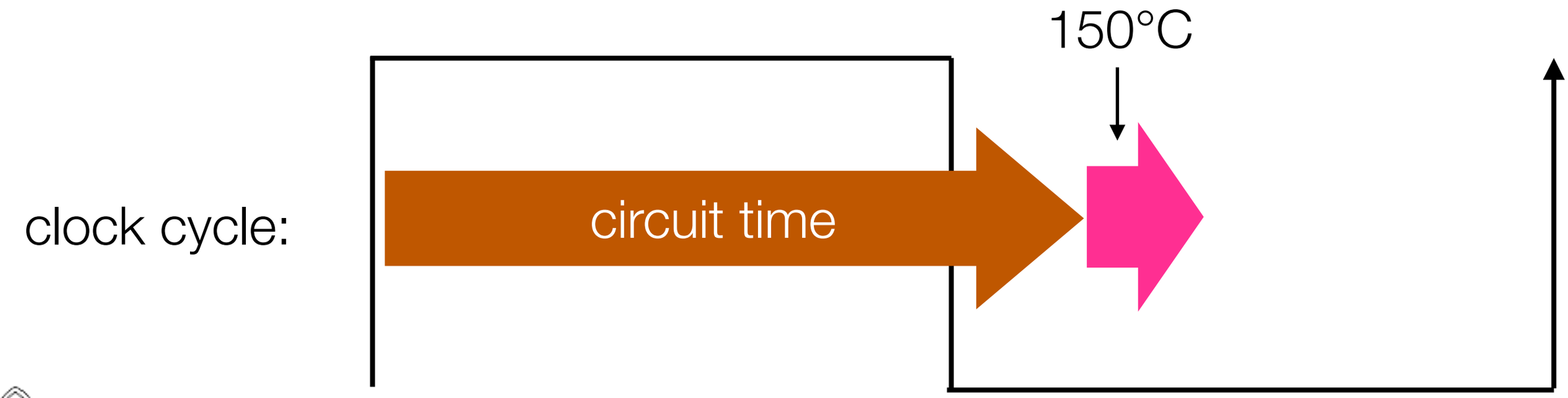

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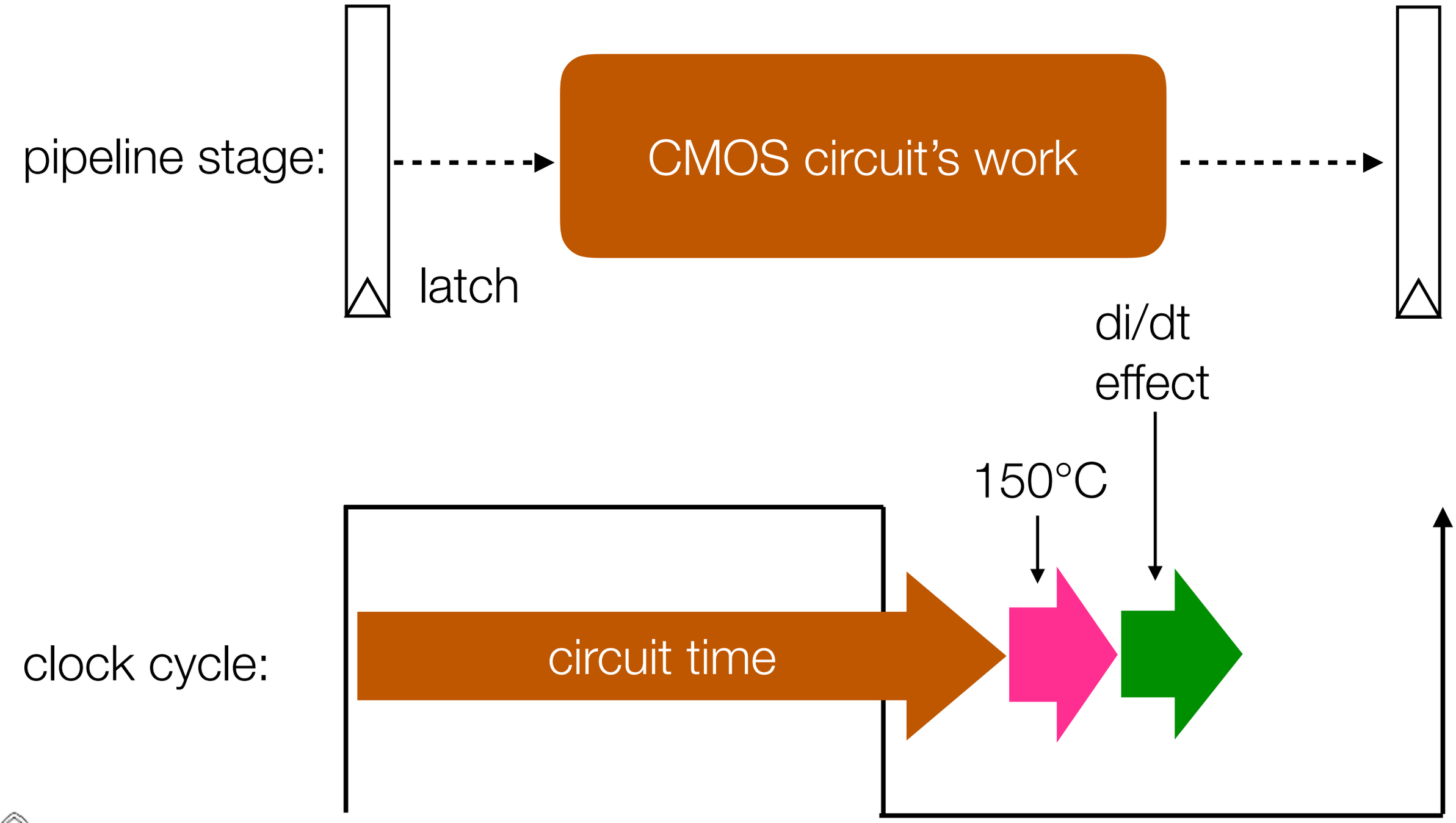

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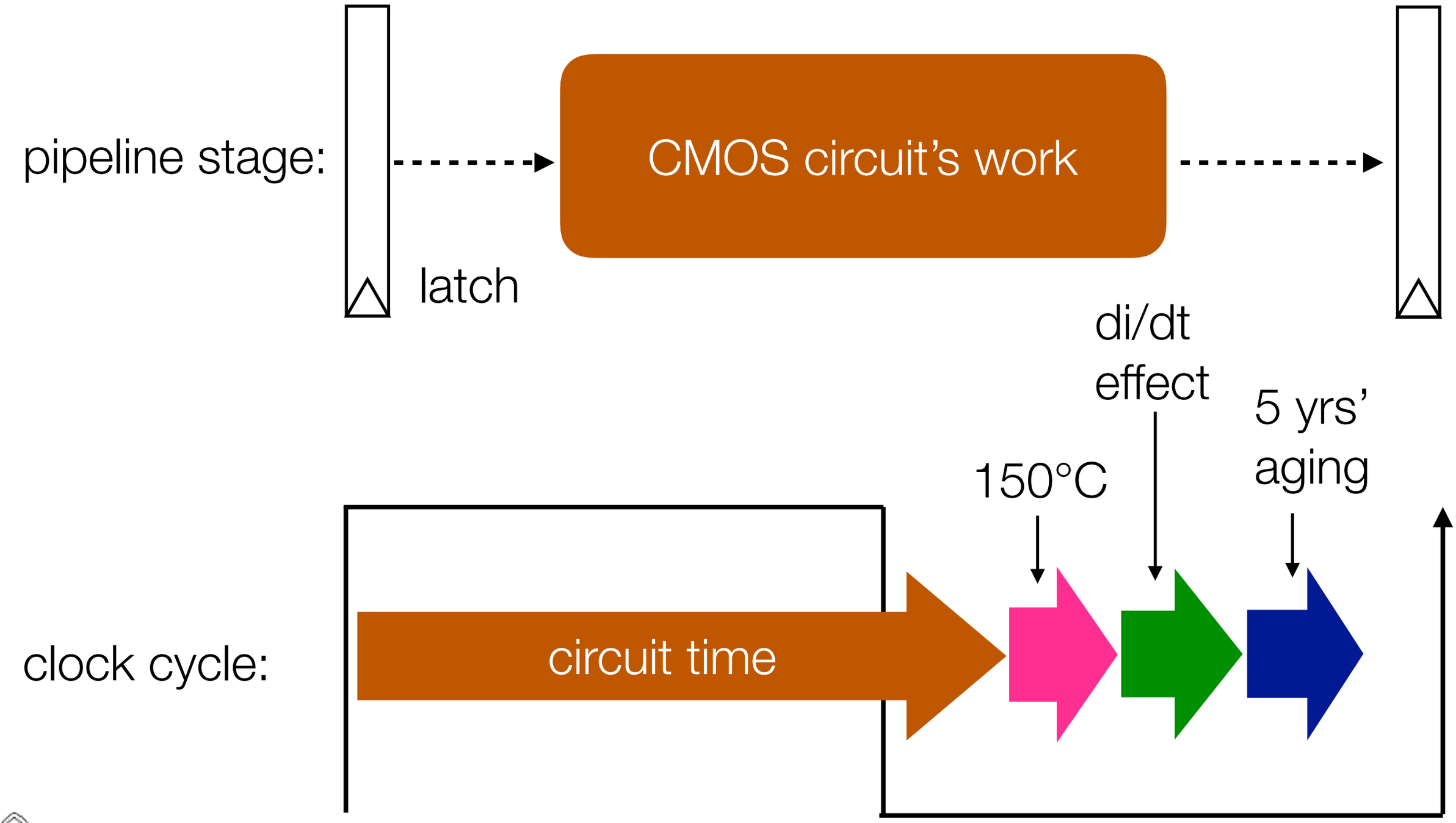

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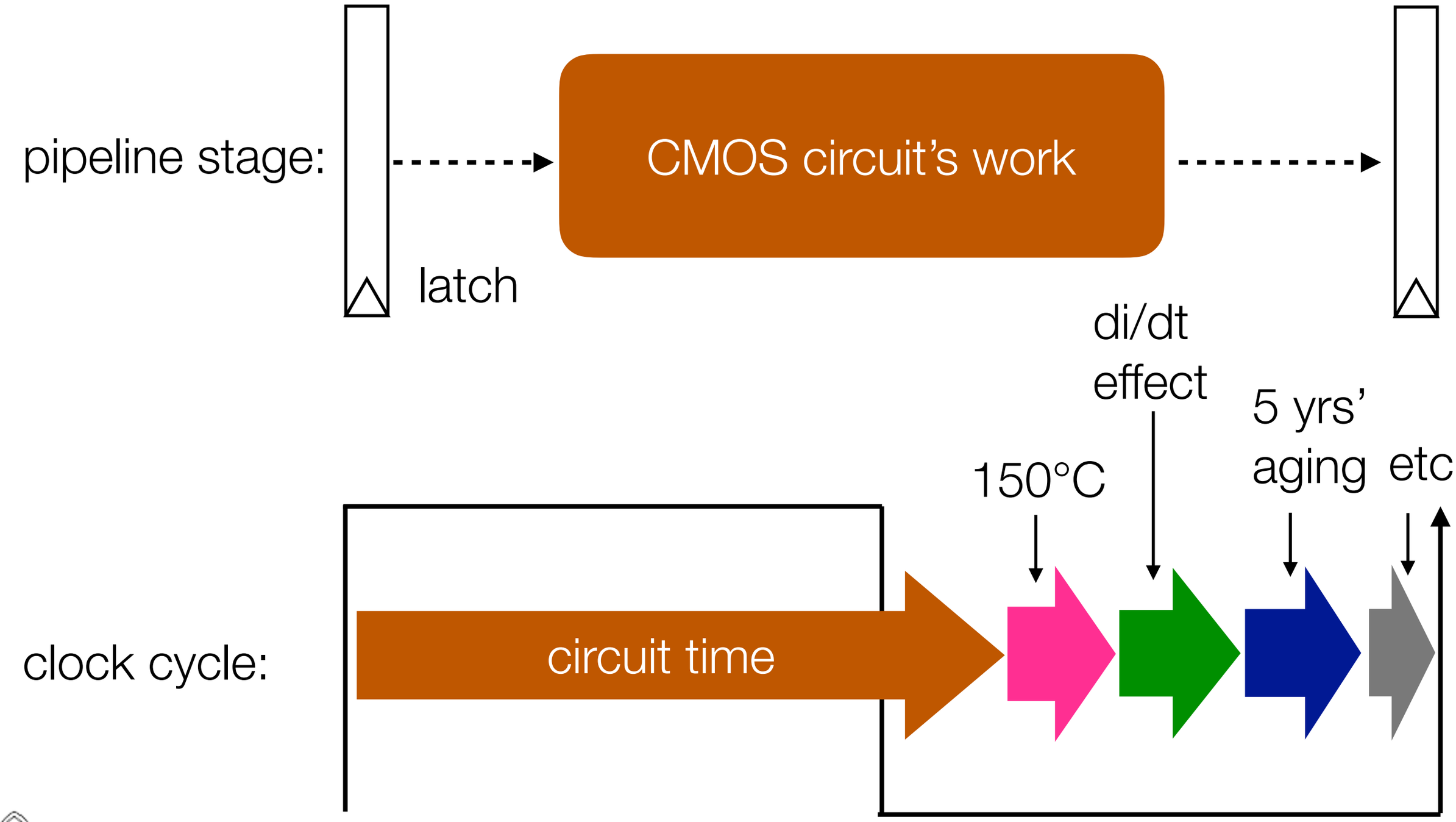

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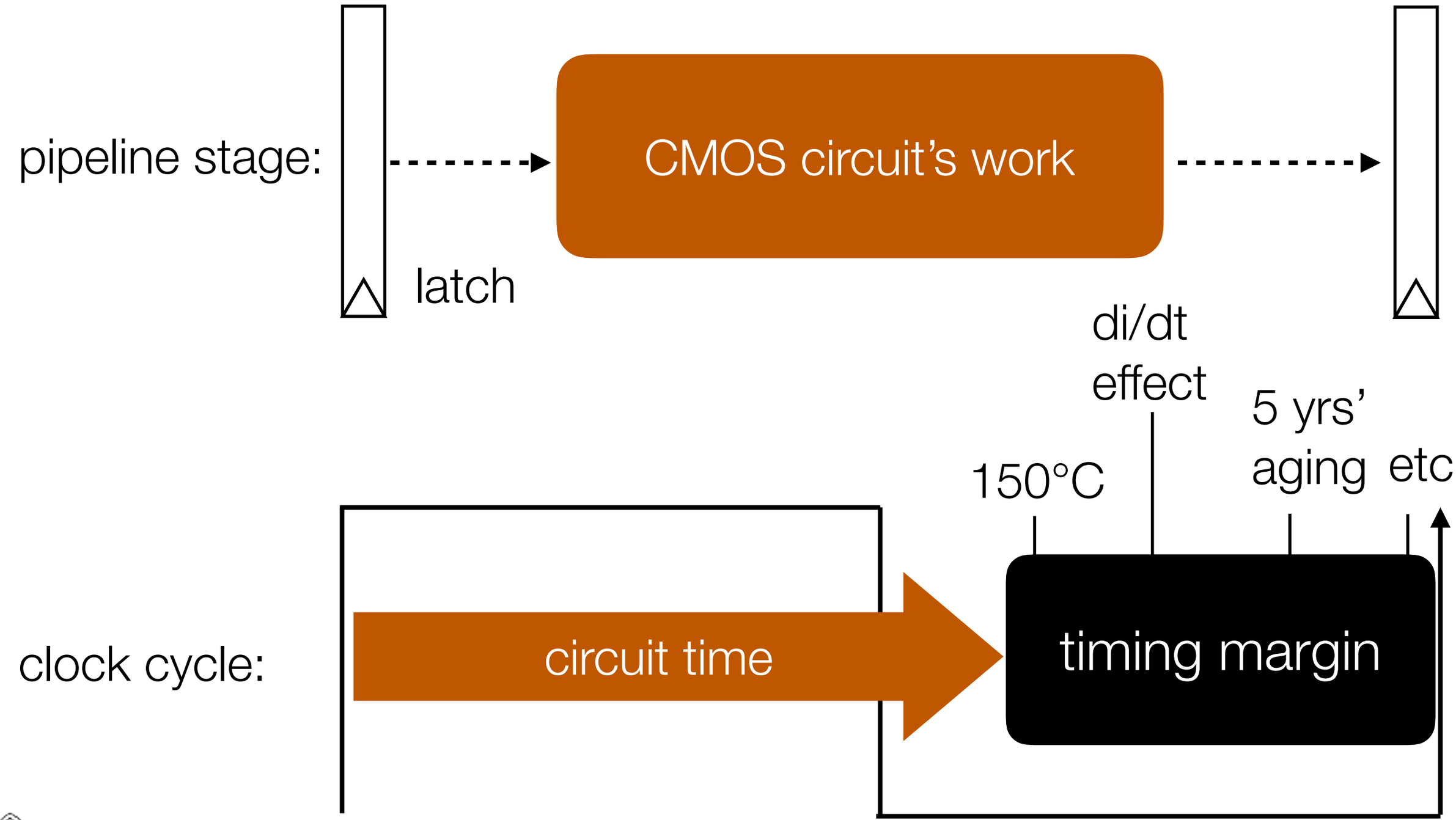

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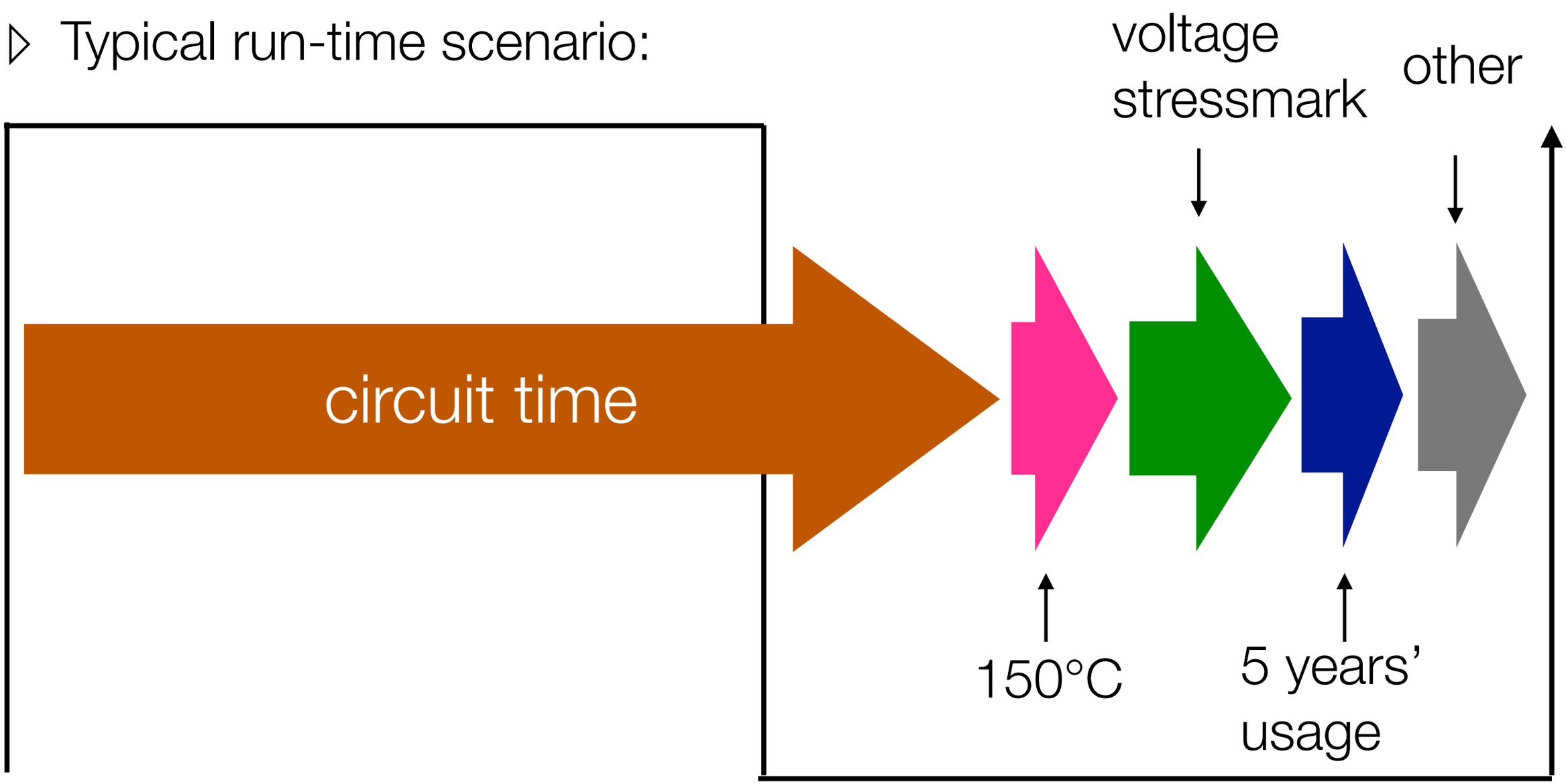

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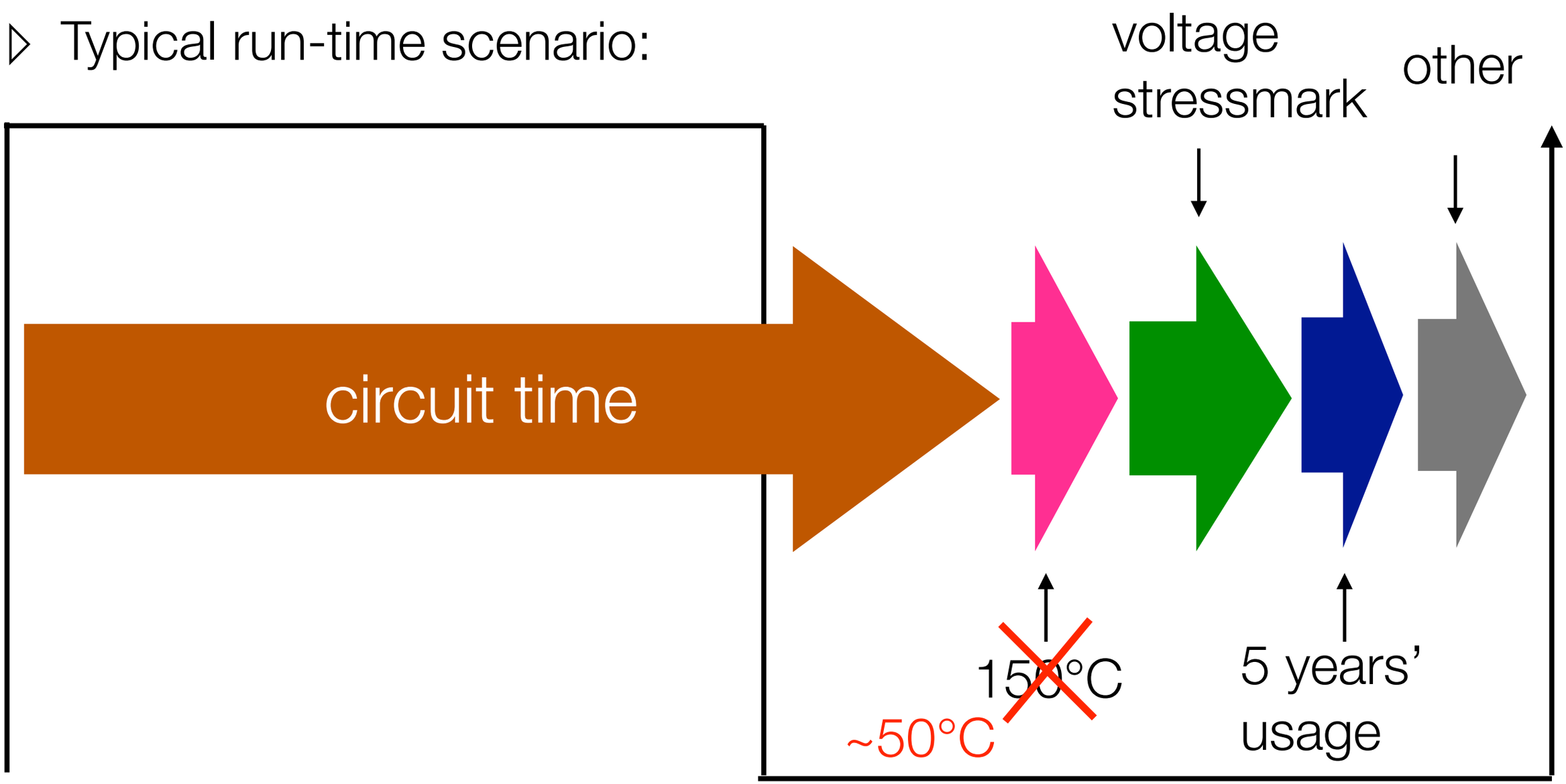

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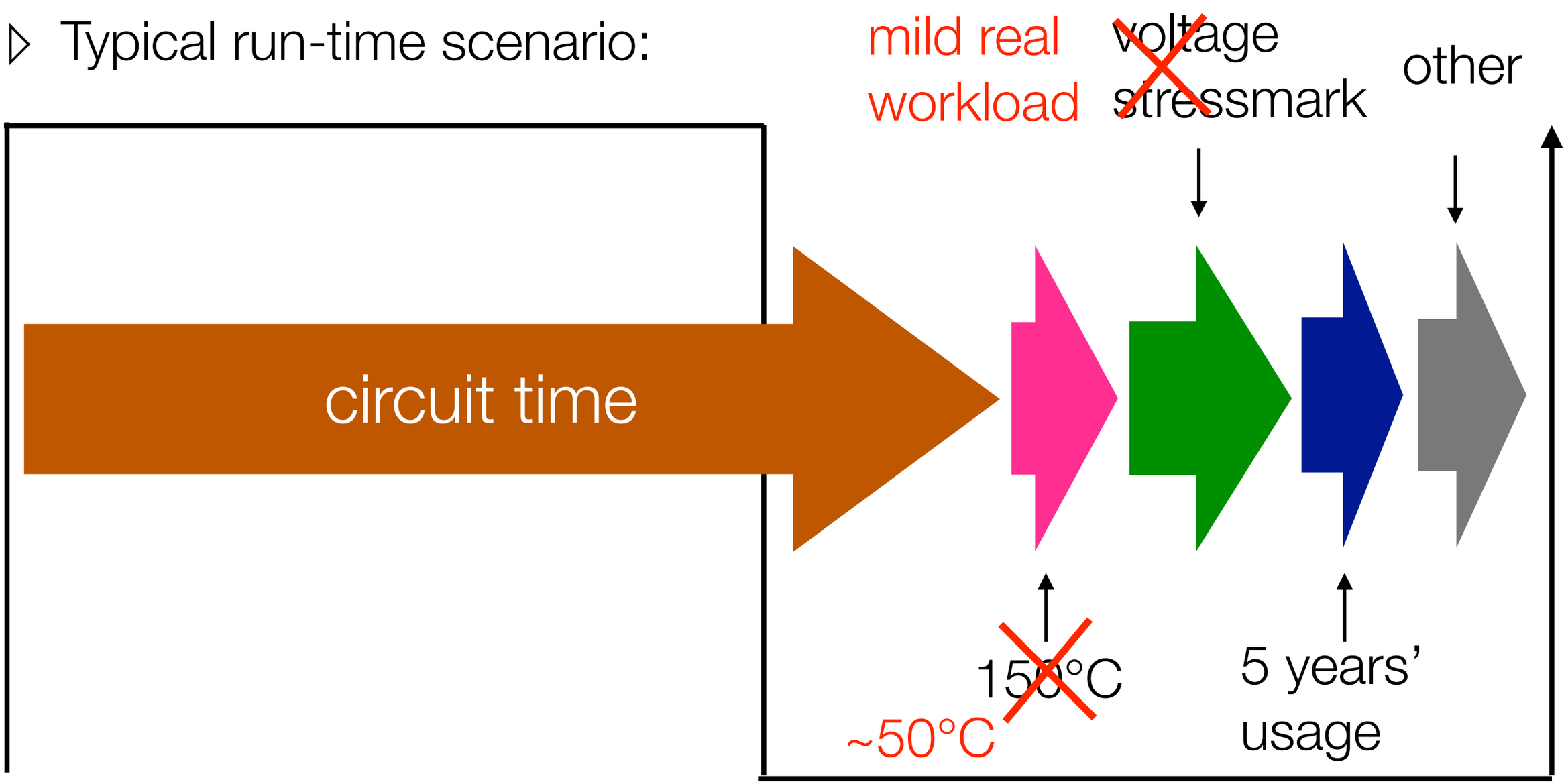

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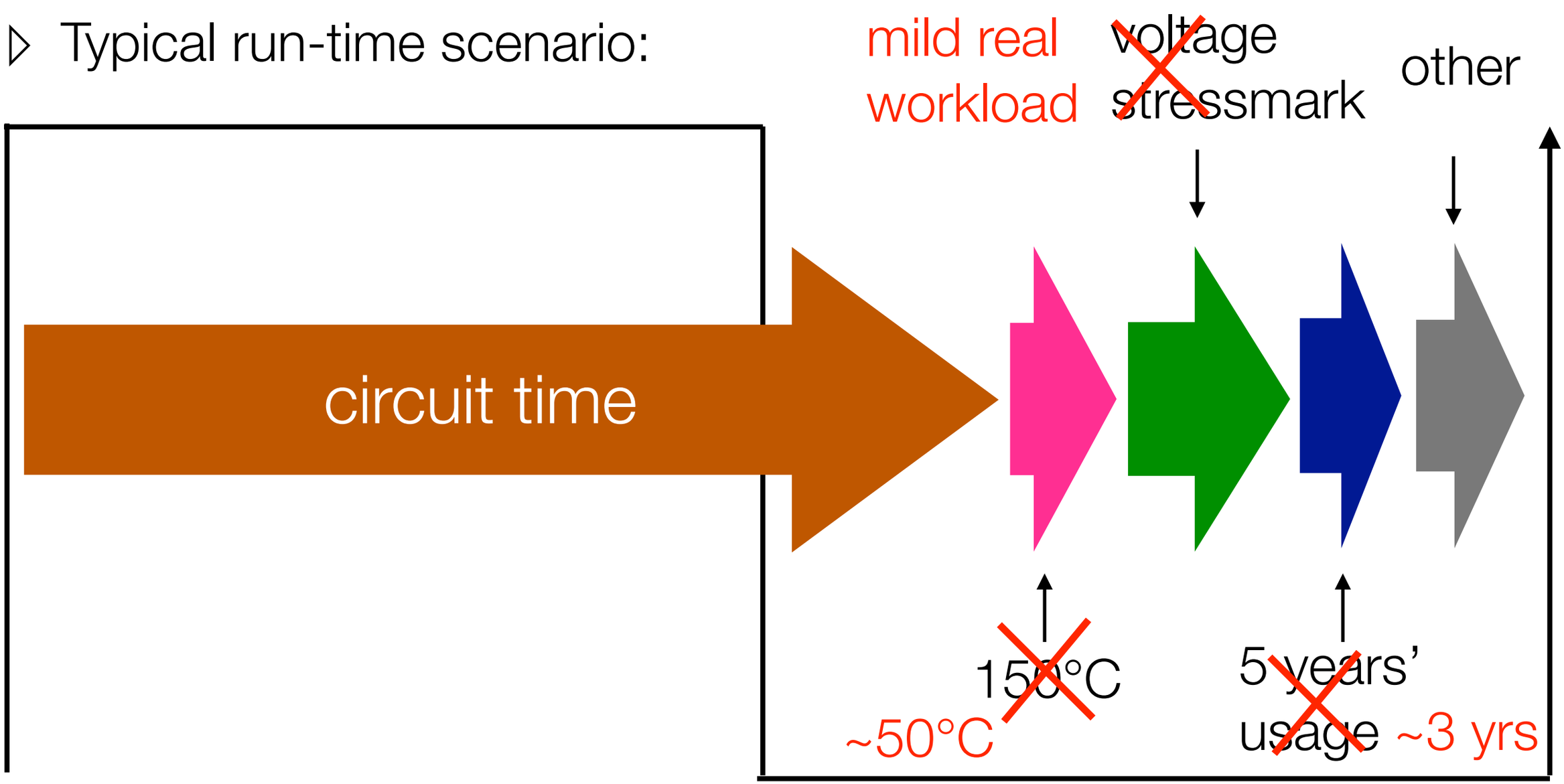

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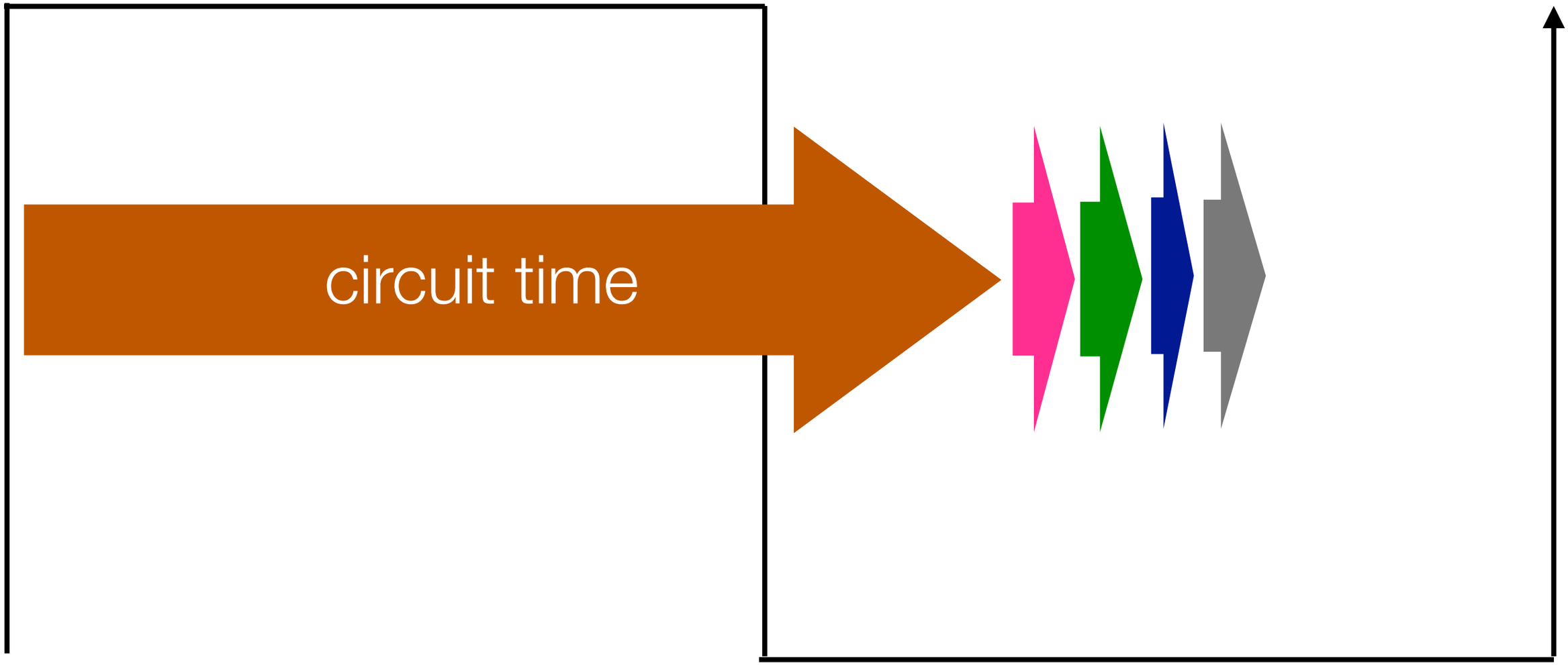

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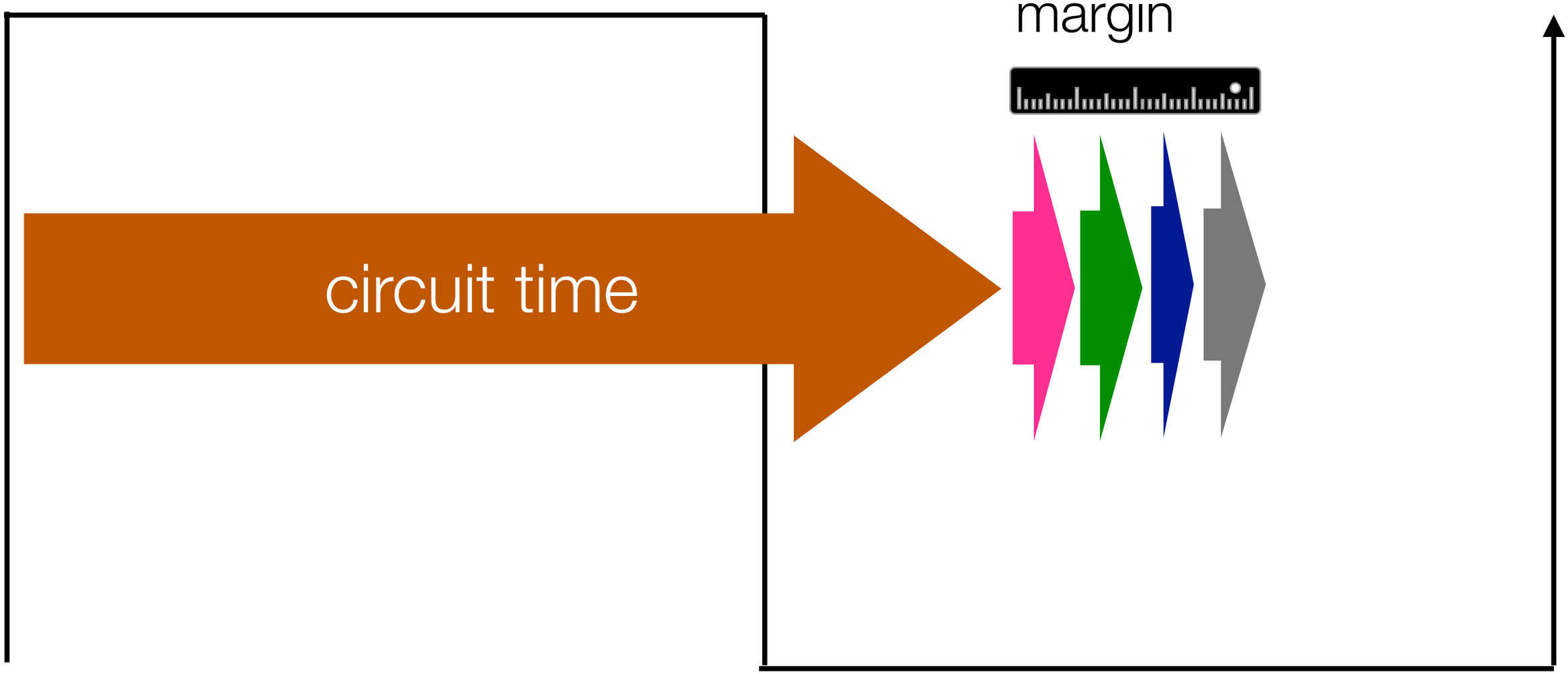

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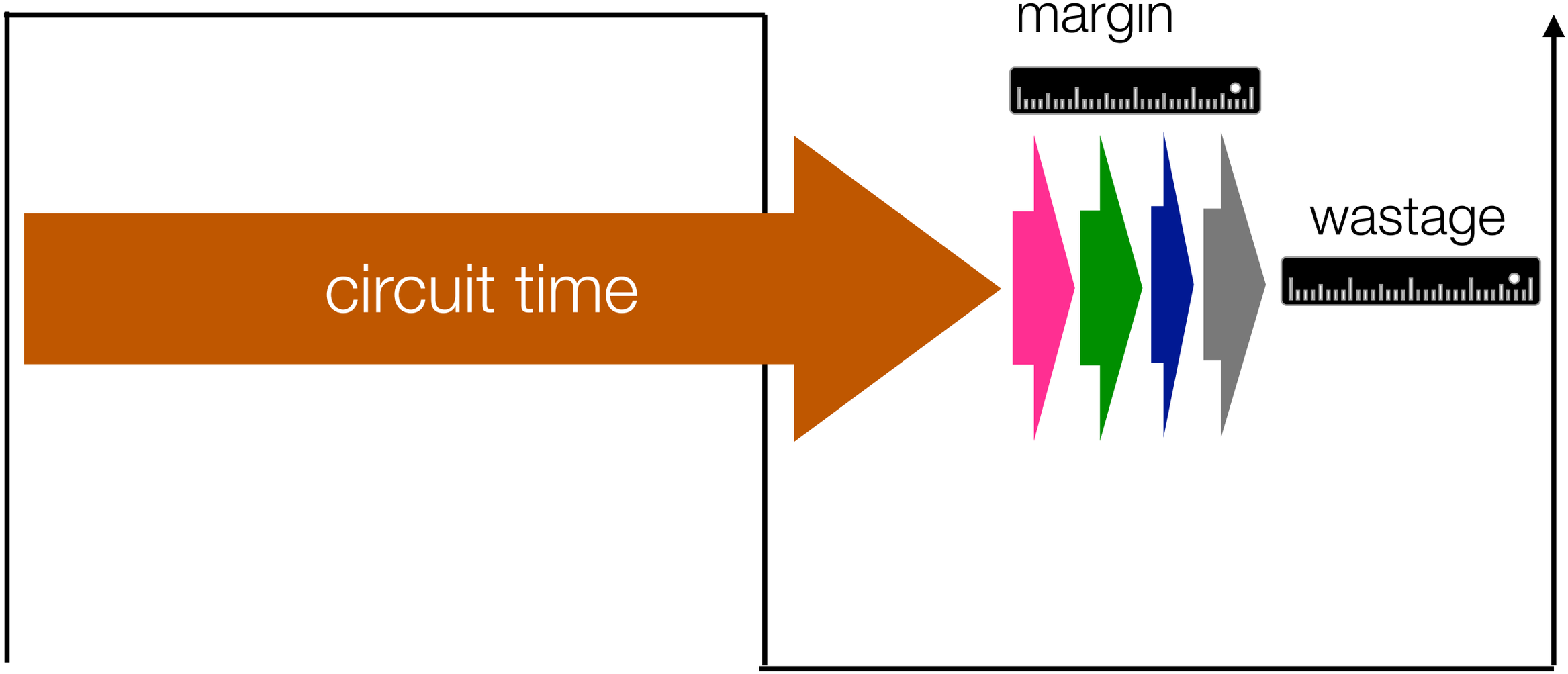
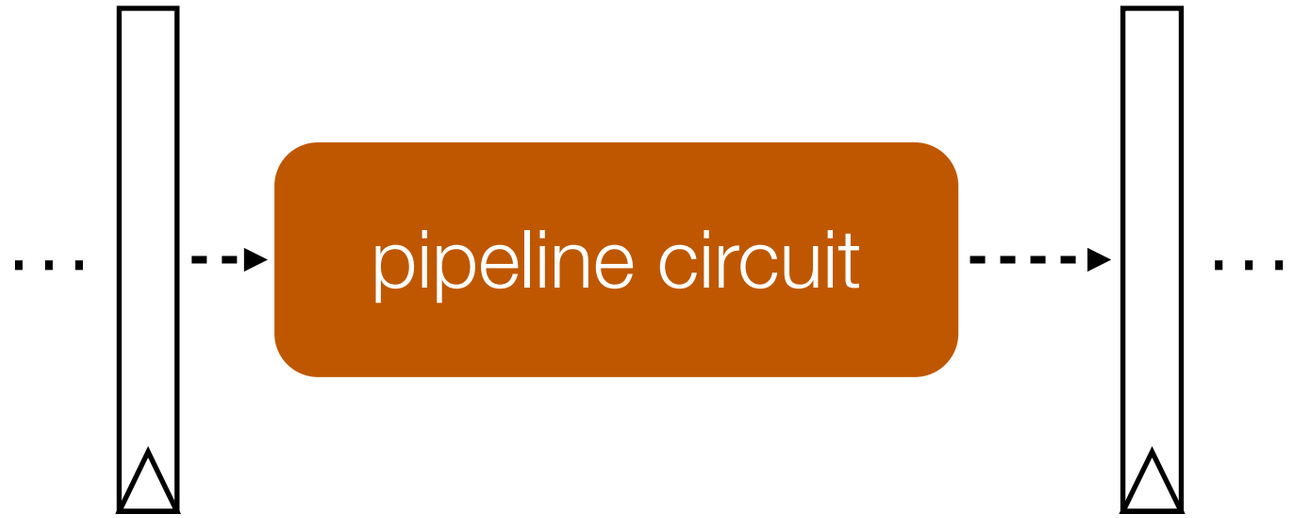


Active Timing Margin: Dynamically Provide Just Enough Margin



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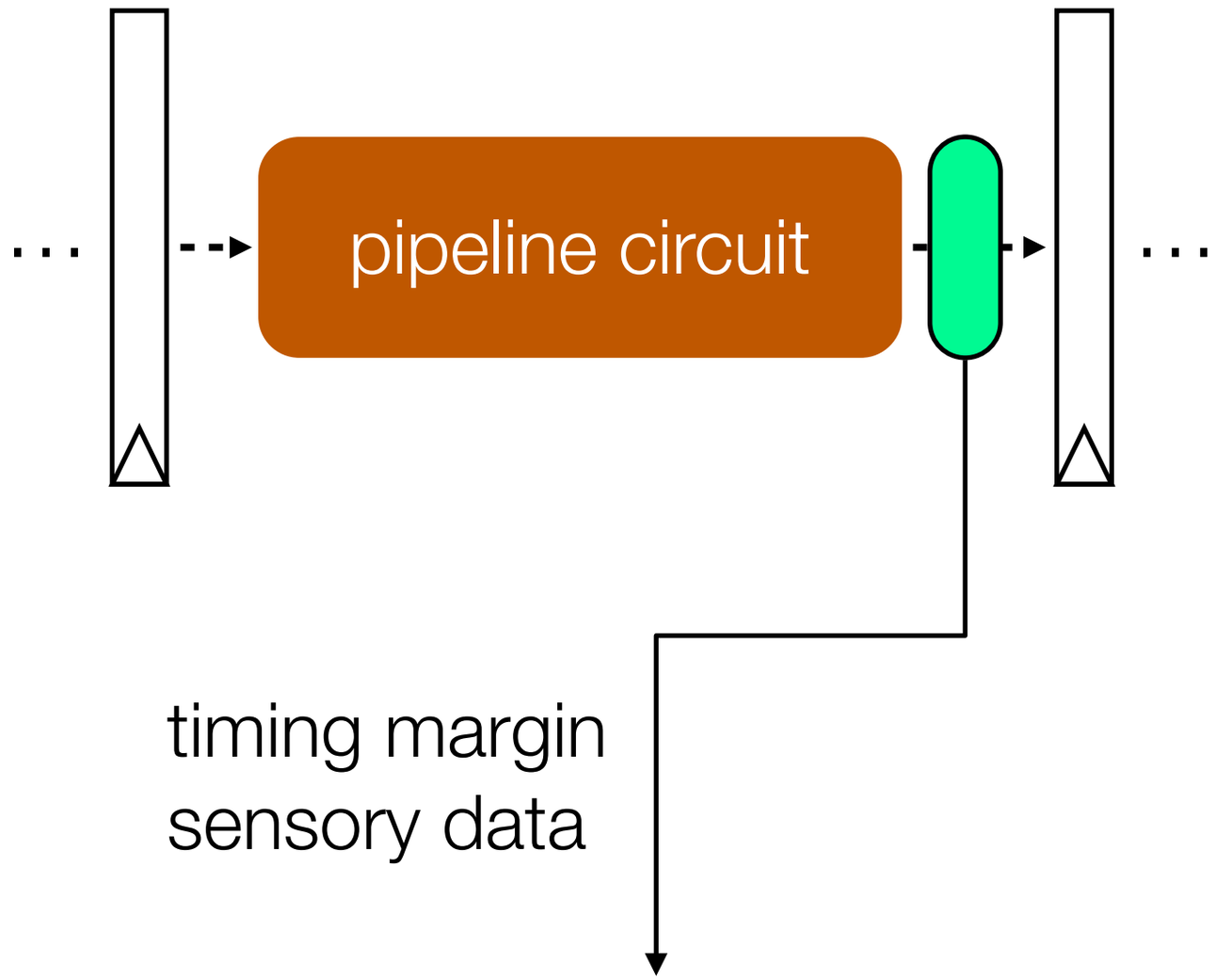

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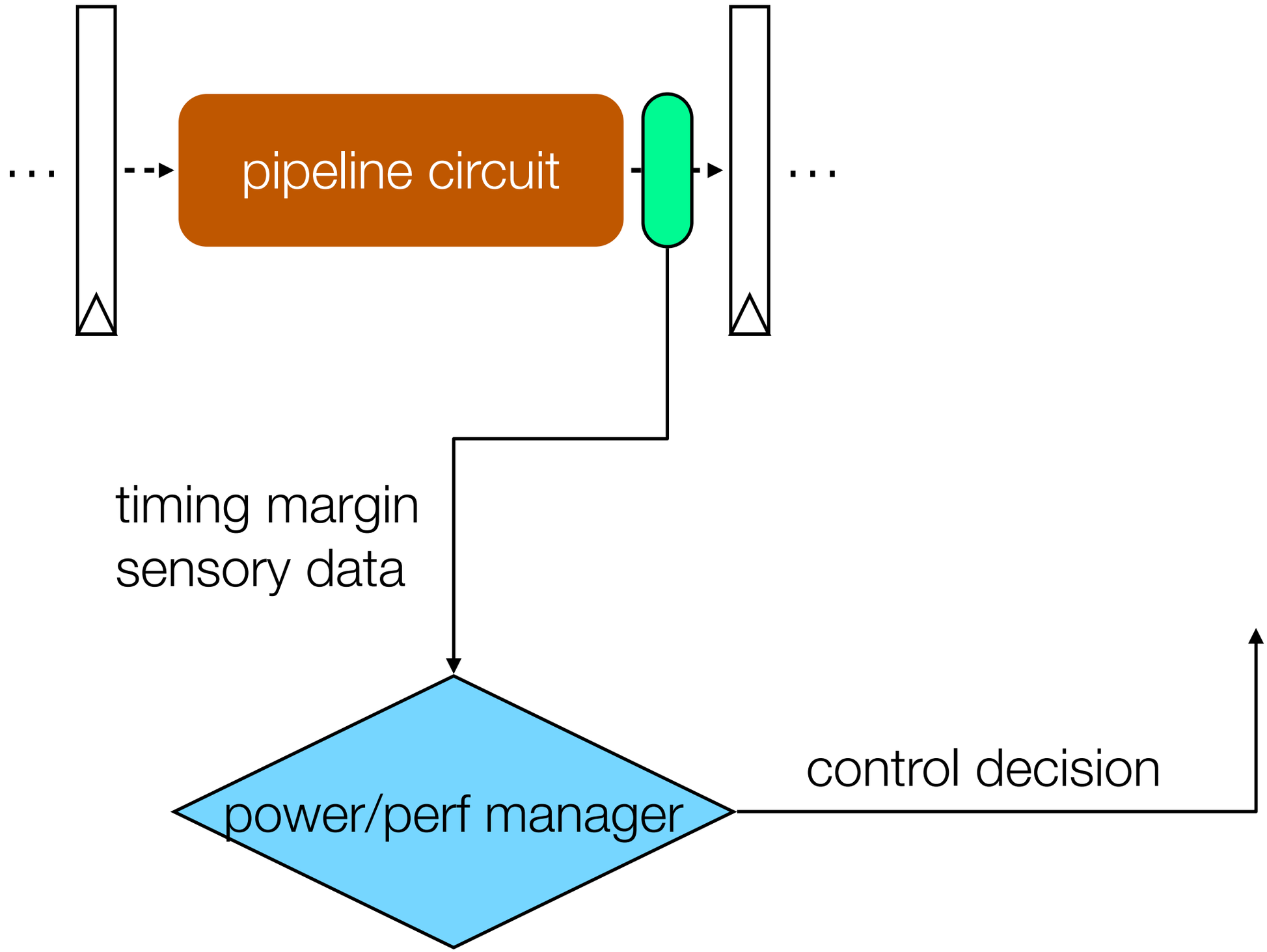

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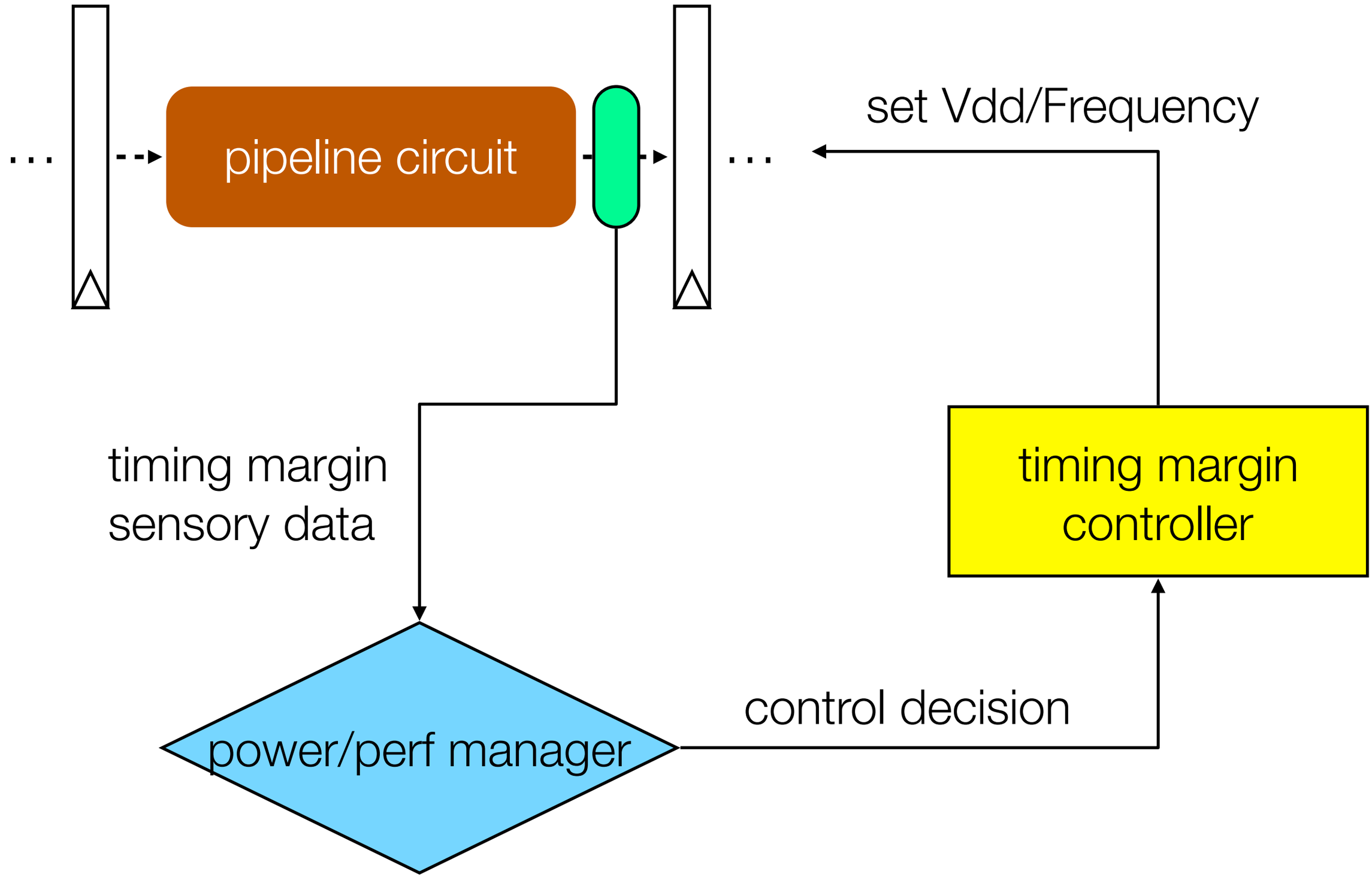

Active Timing Margin (ATM)

Software

Hardware

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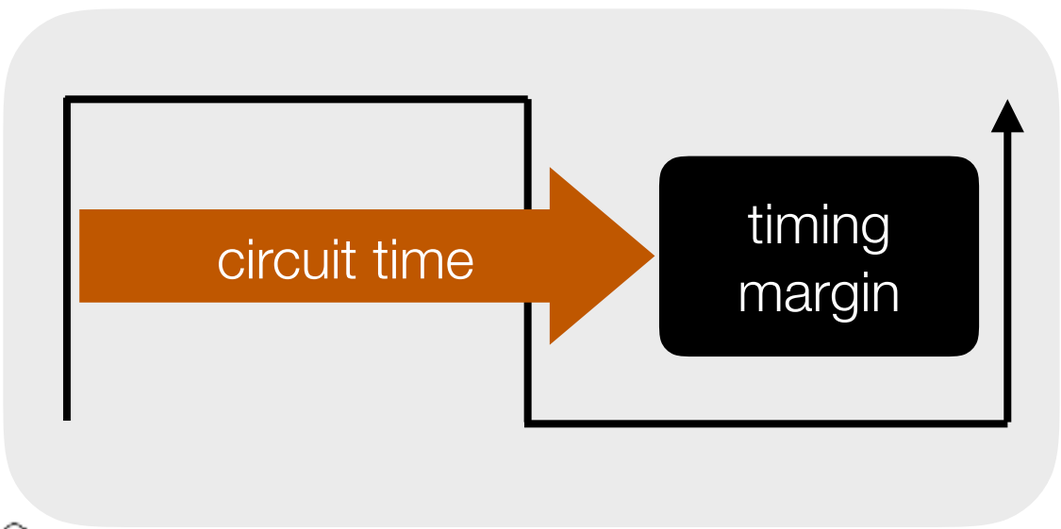
Hardware



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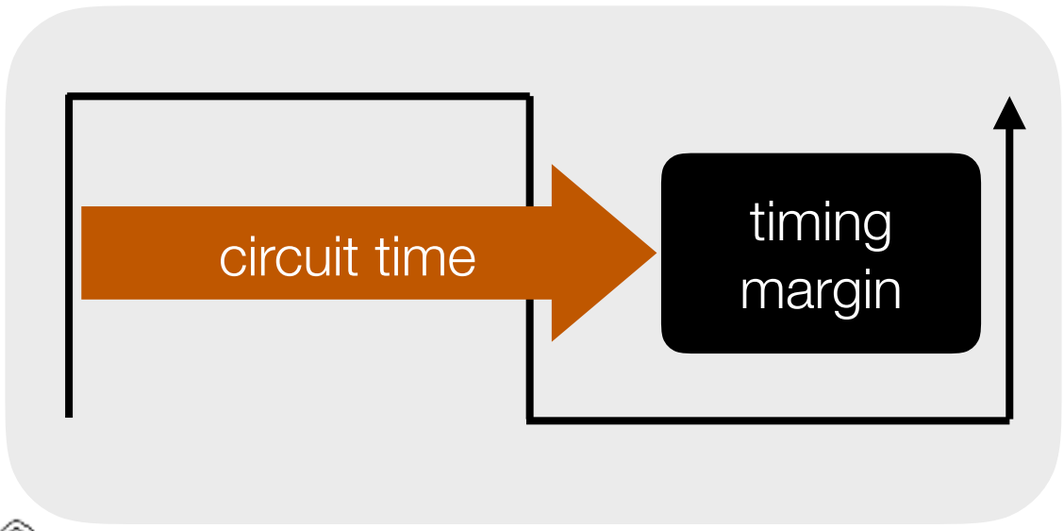
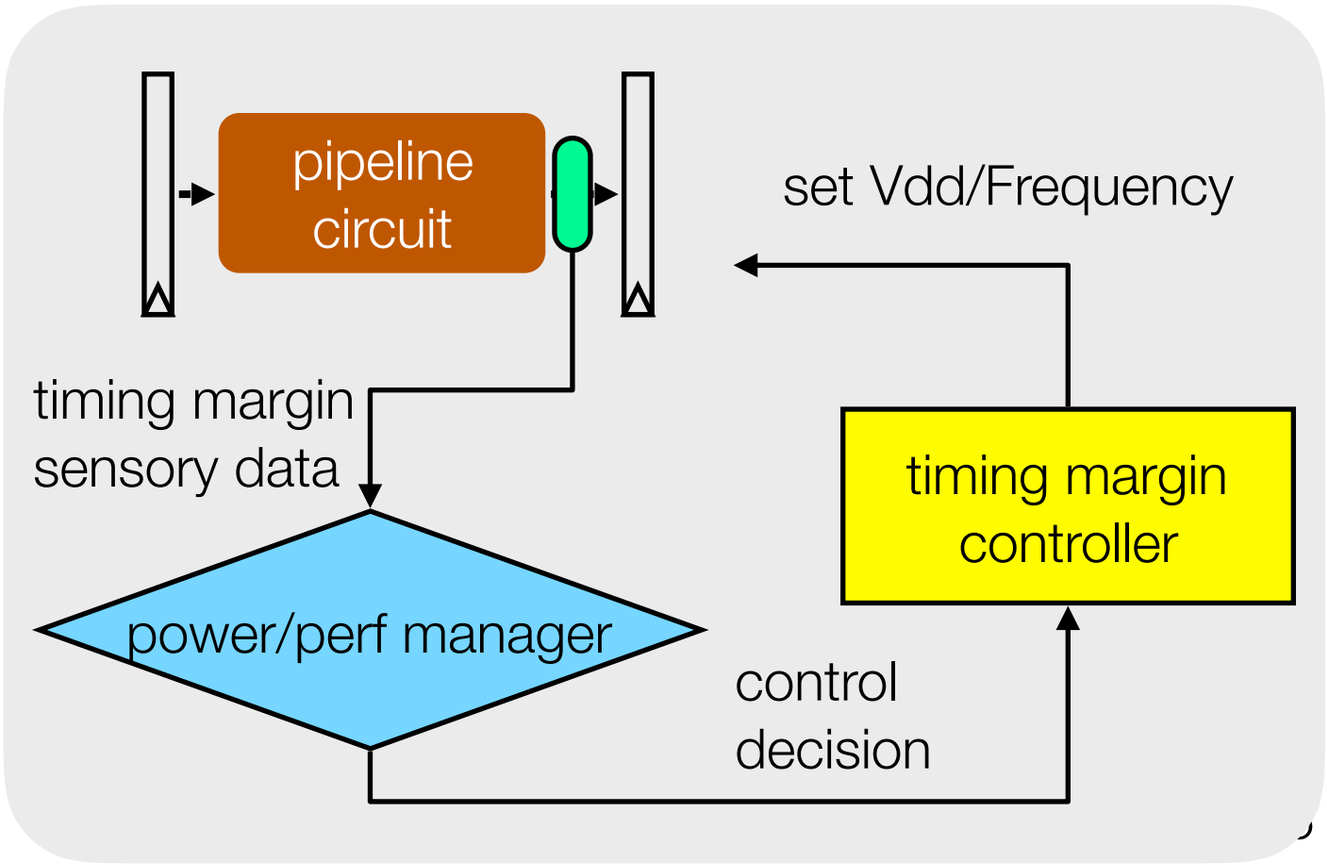


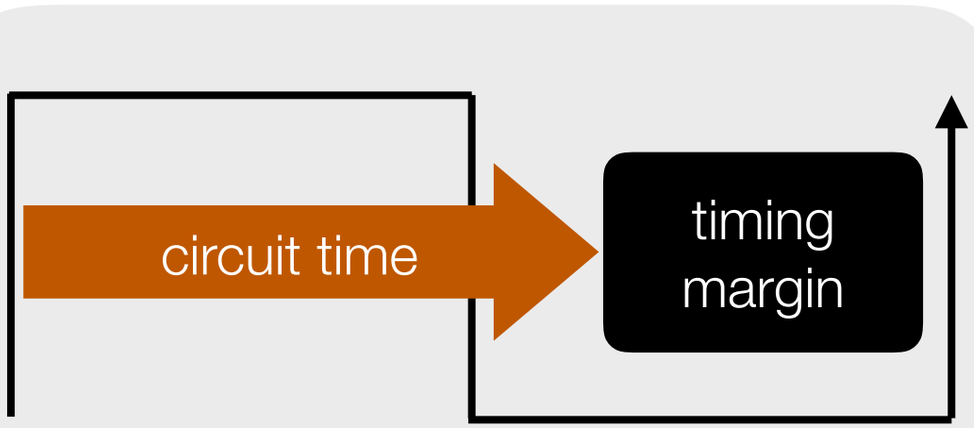


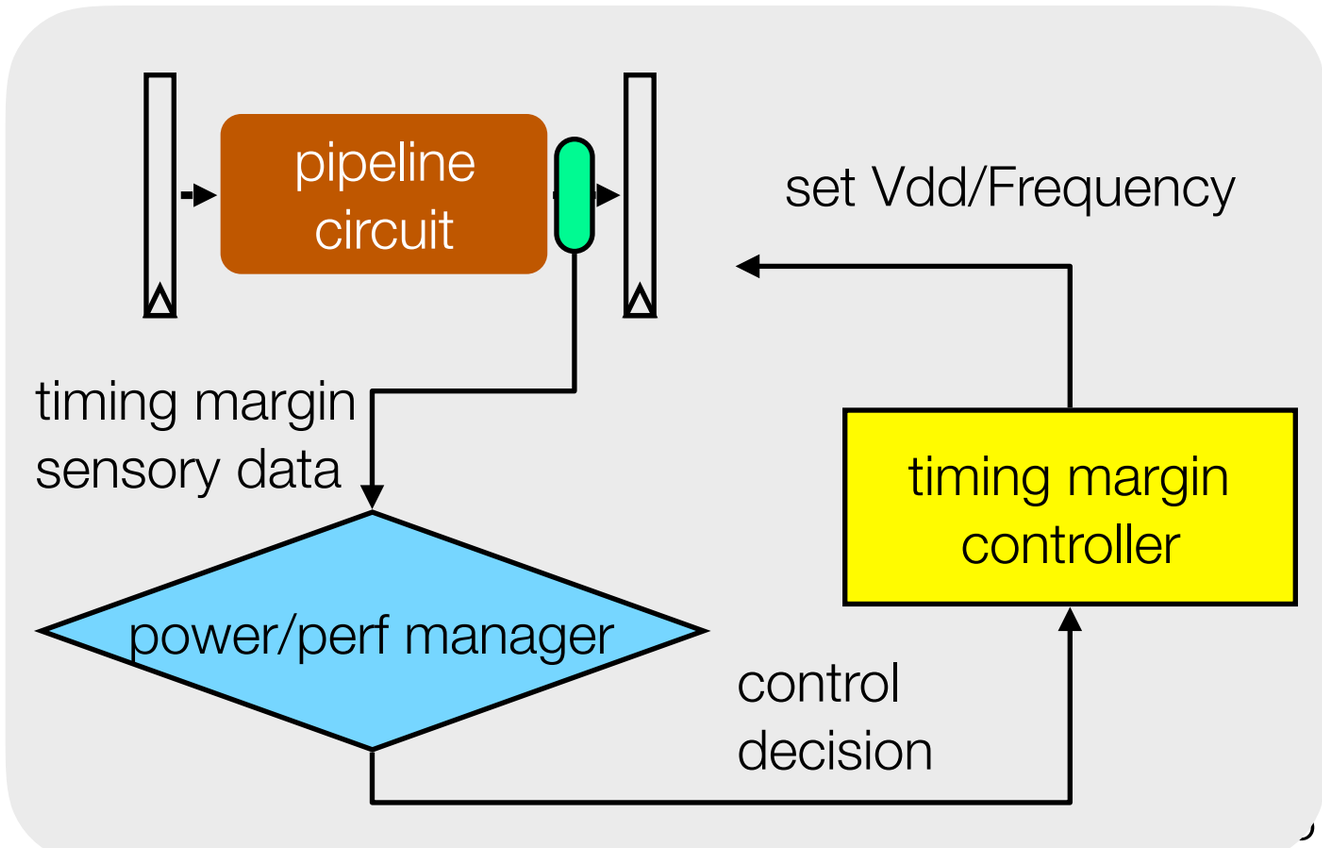
Active Timing Margin (ATM)

Software

Runs Anything!

Hardware





Active Timing Margin (ATM) — A Free Meal

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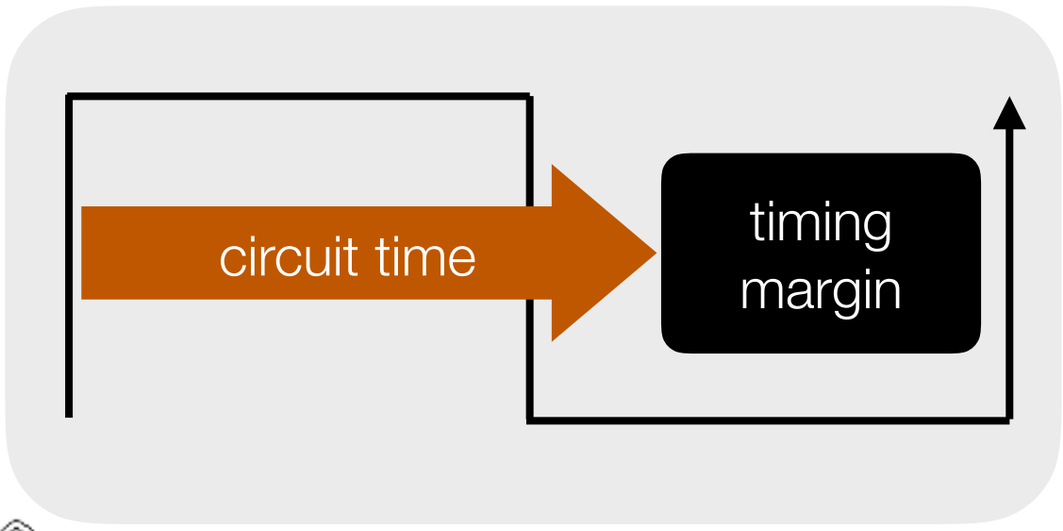
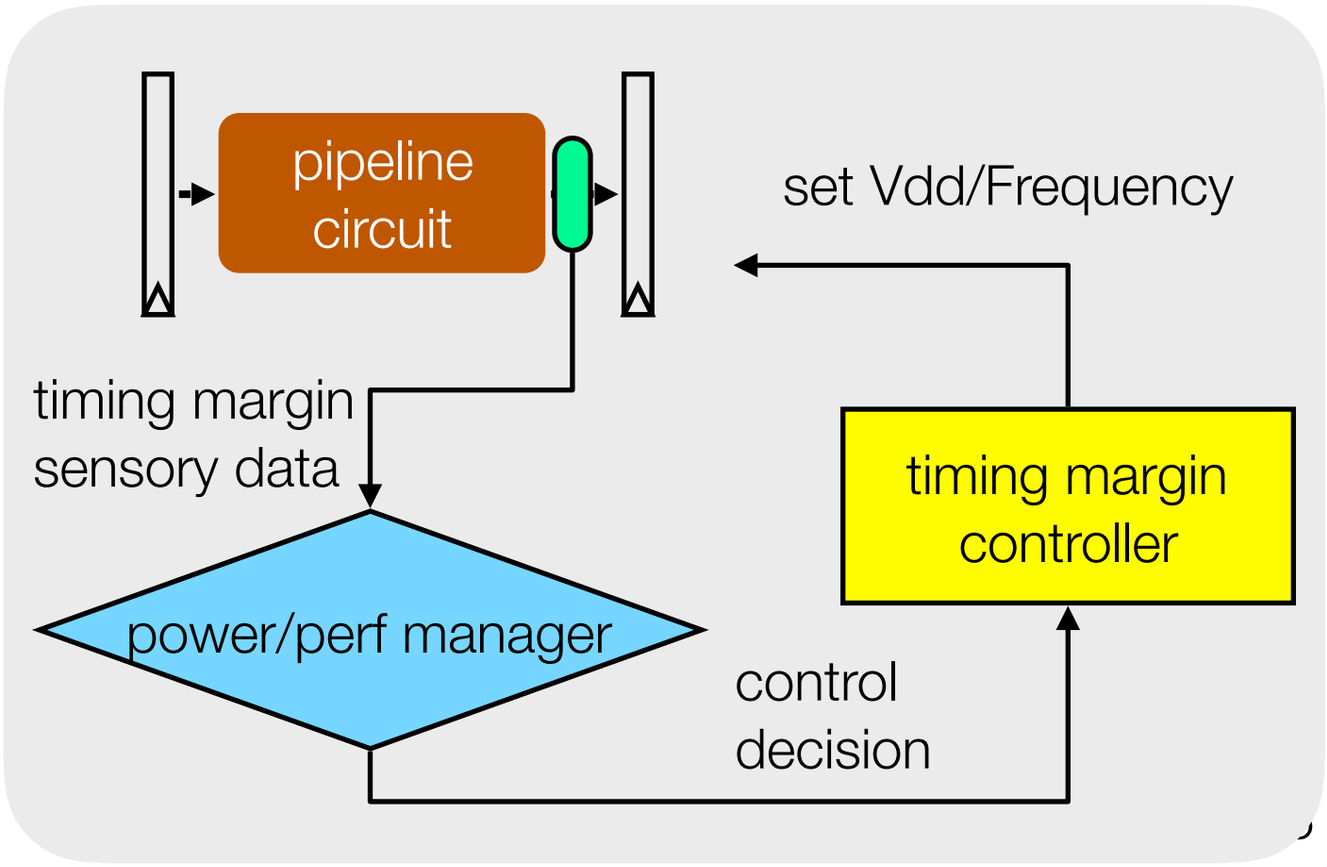
Runs Anything!

Hardware





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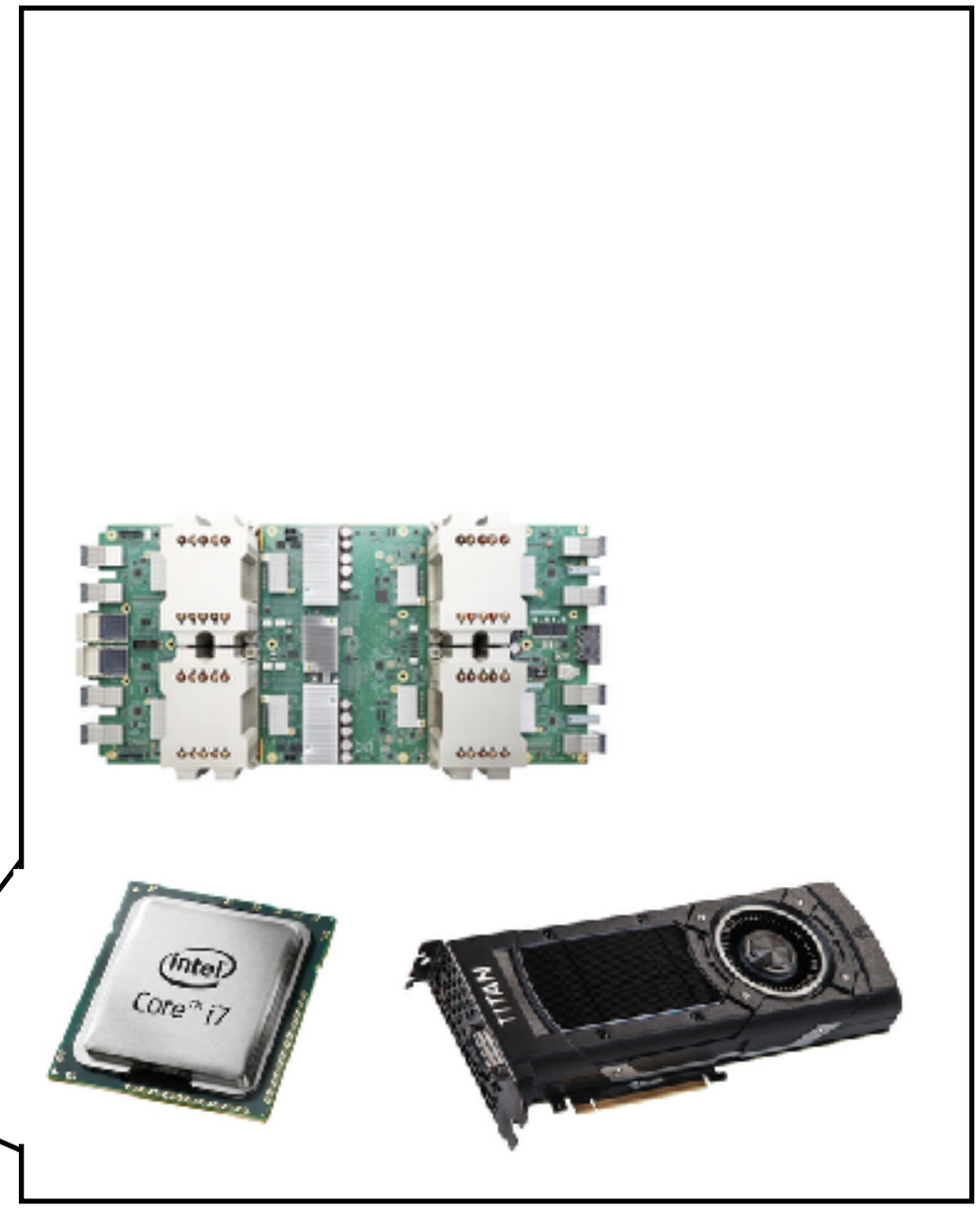

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Problems of Existing ATMs - (Has to) Ignore Variation

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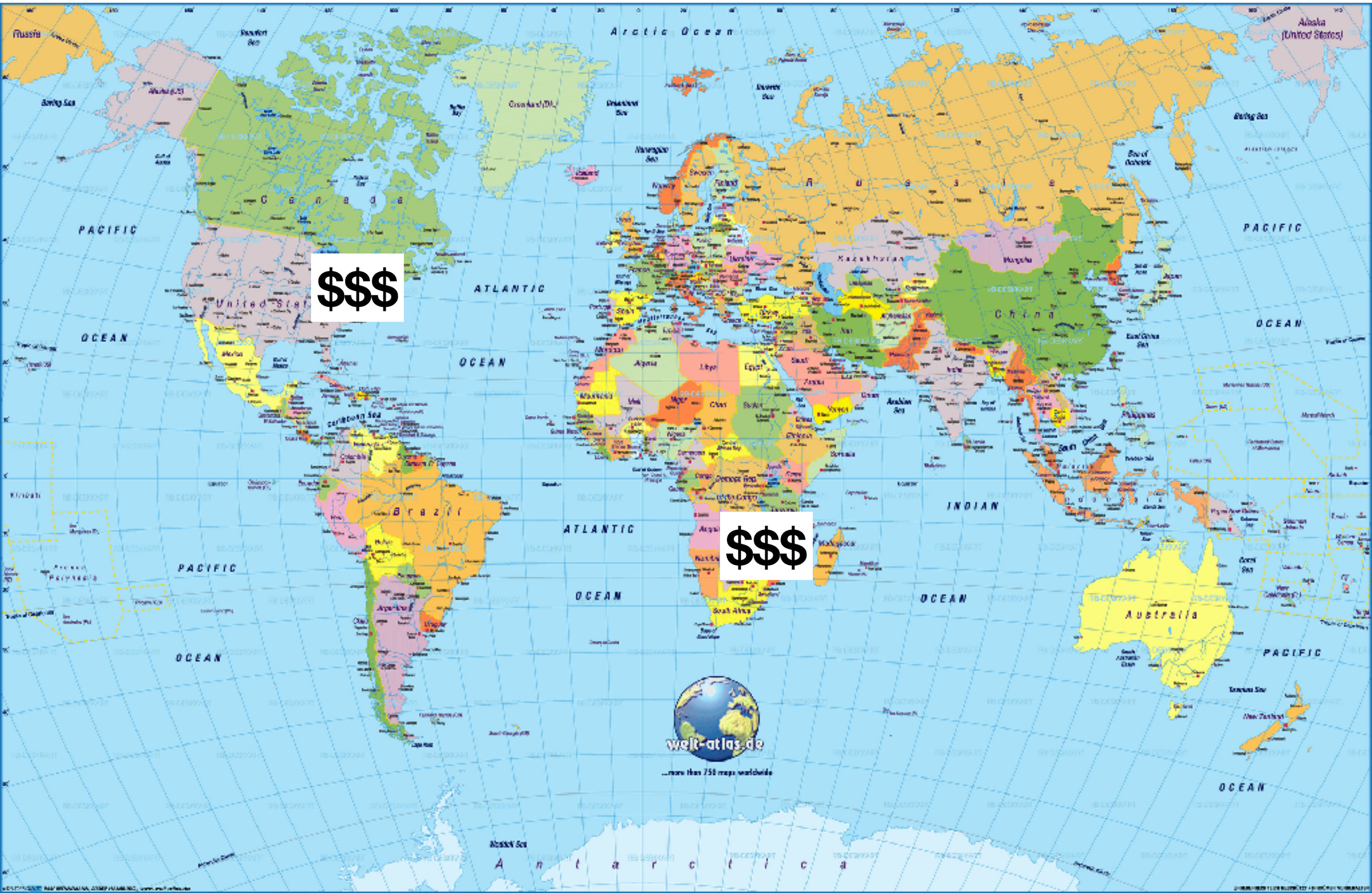

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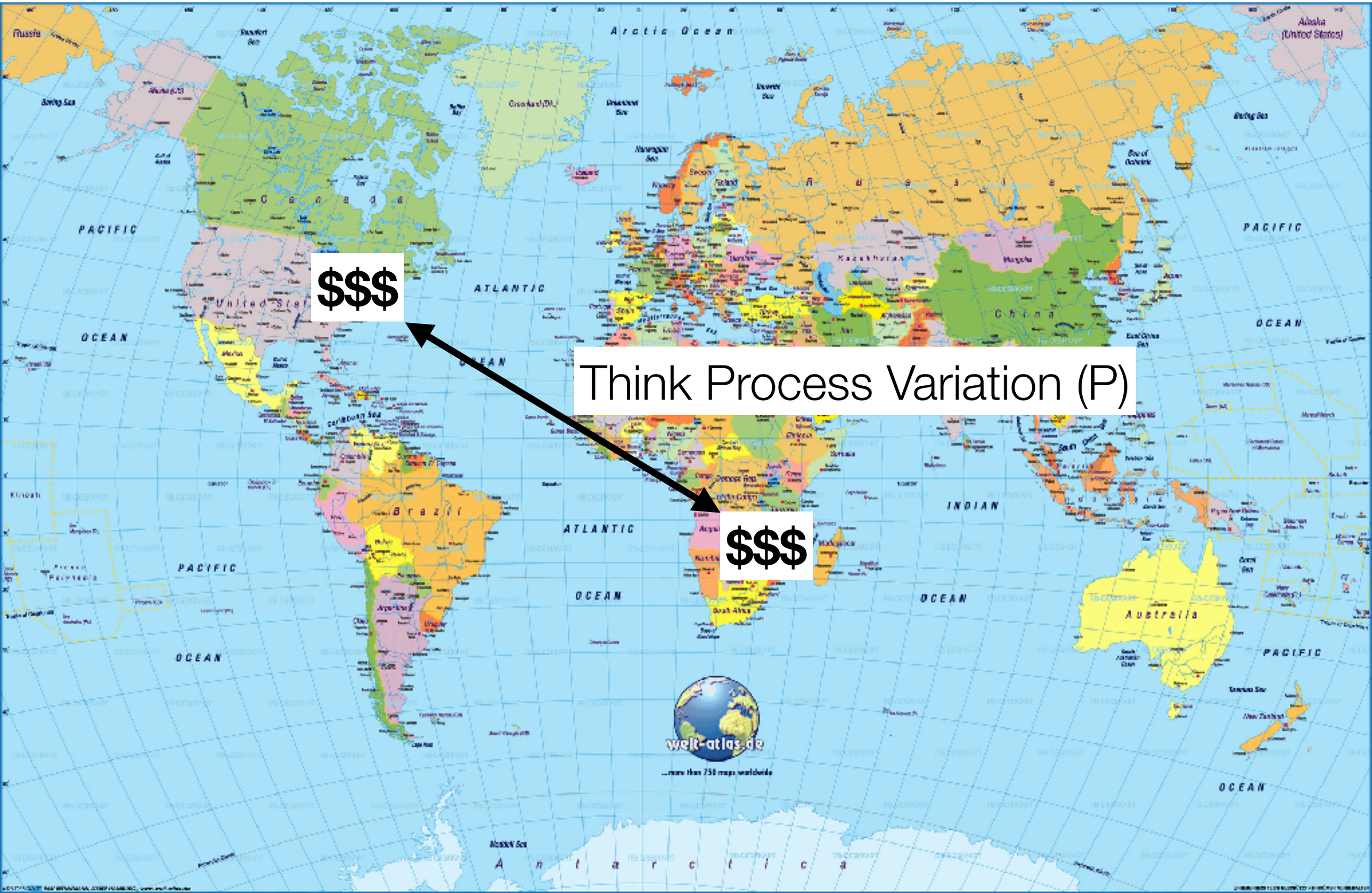
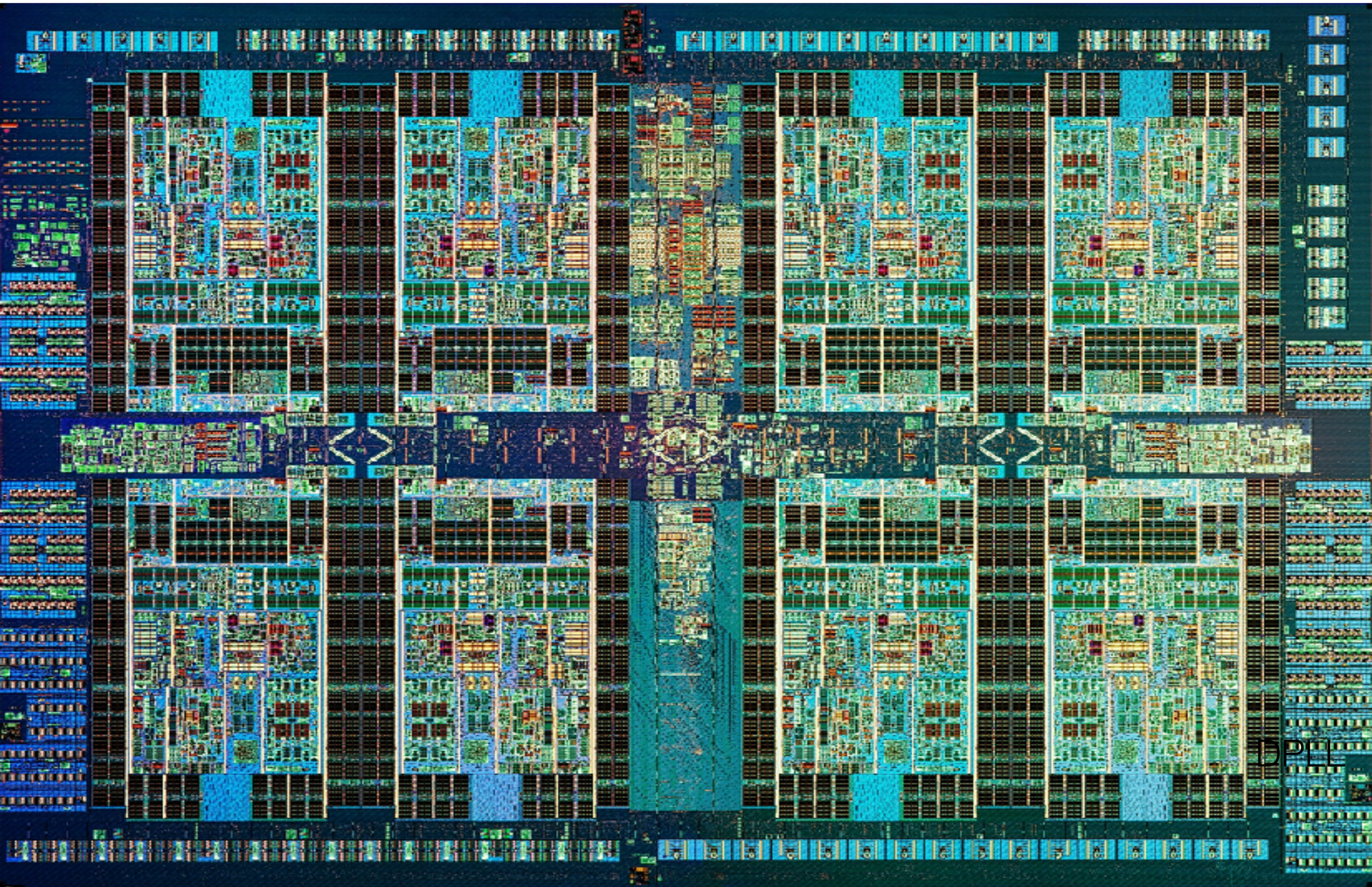


Executive Summary

- Fine-tune core-level ATM to **automatically** expose inter-core performance variation

Experimental Setup: IBM® Eight-core POWER7+ x 2



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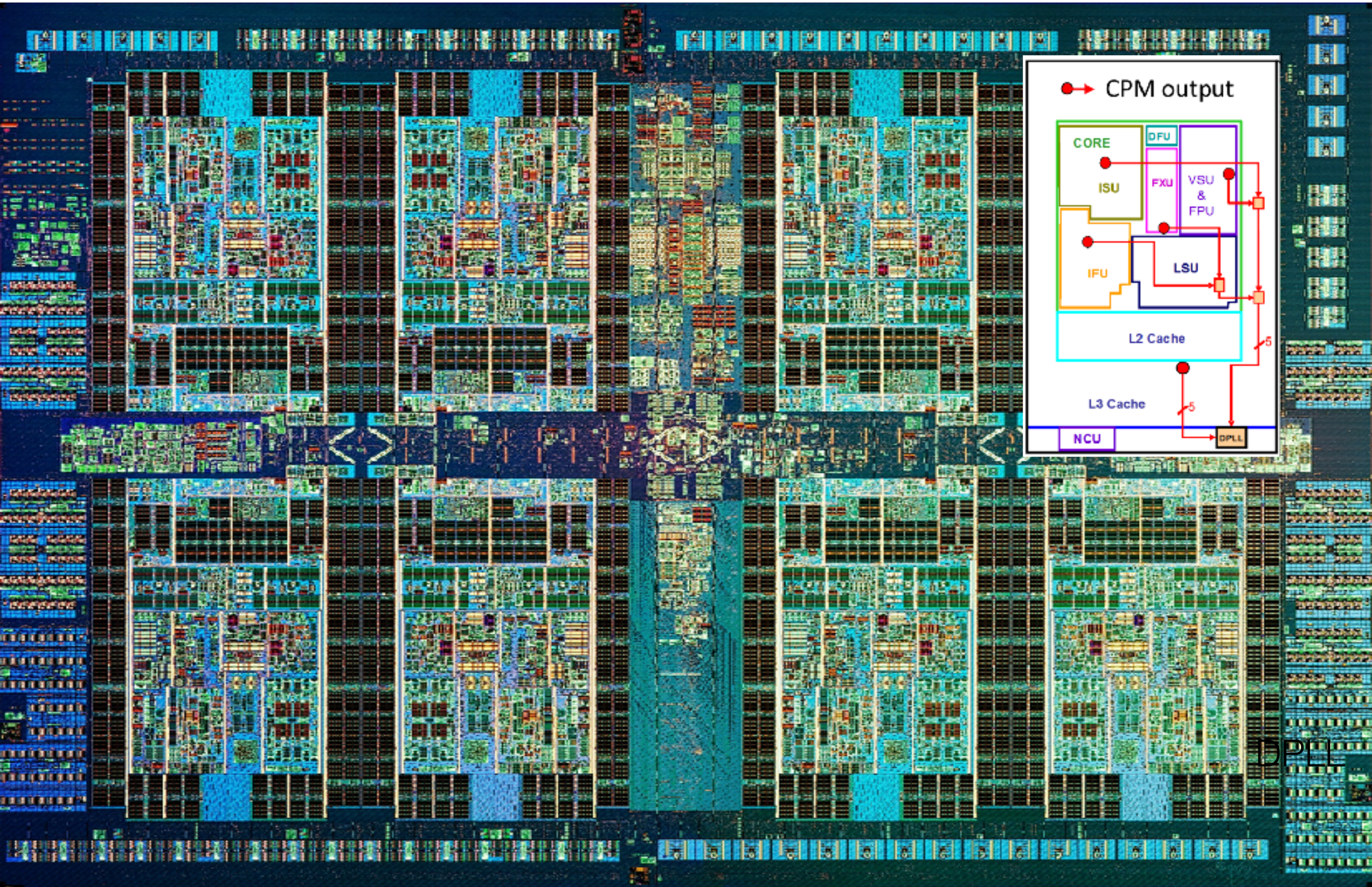
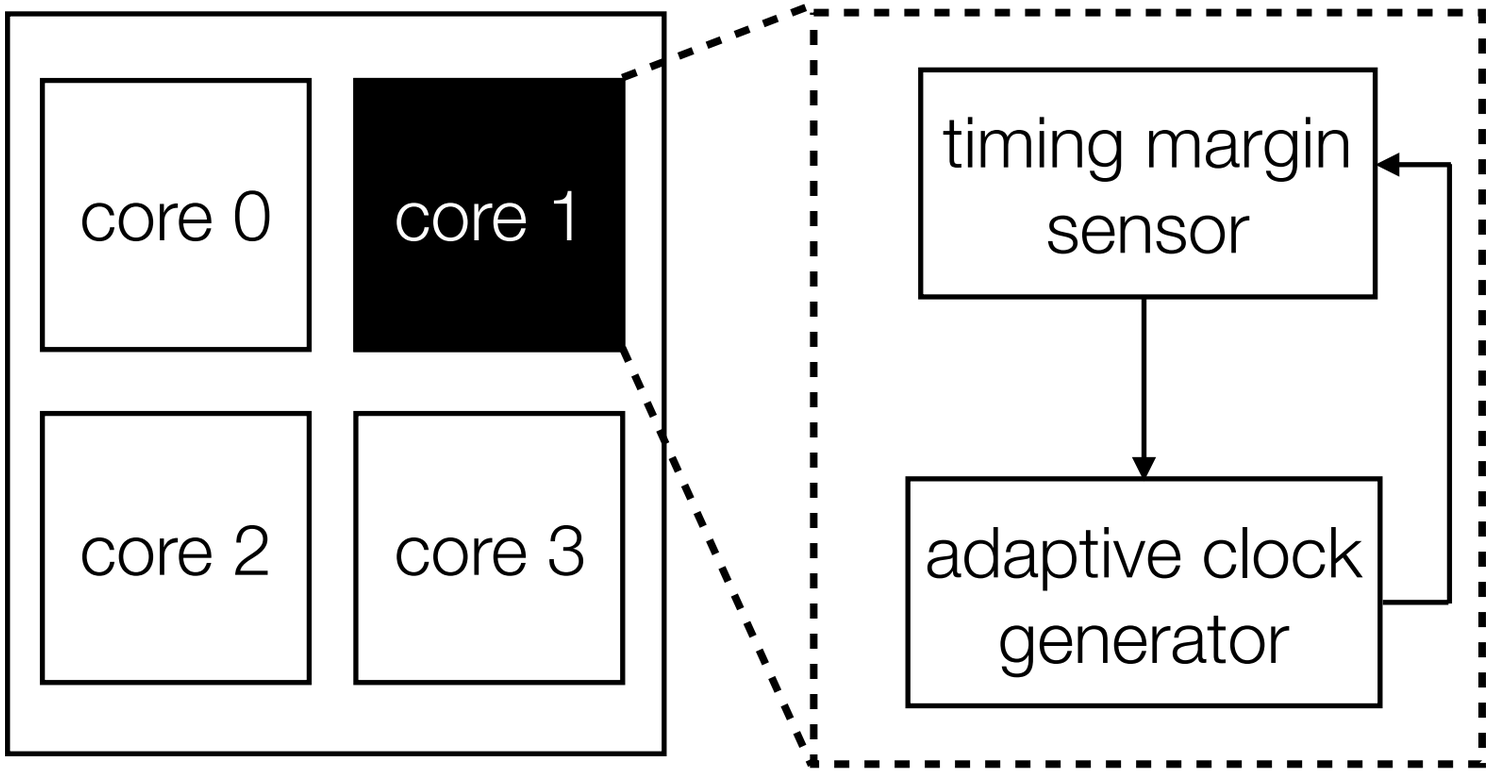


Expose Core-level Performance with ATM



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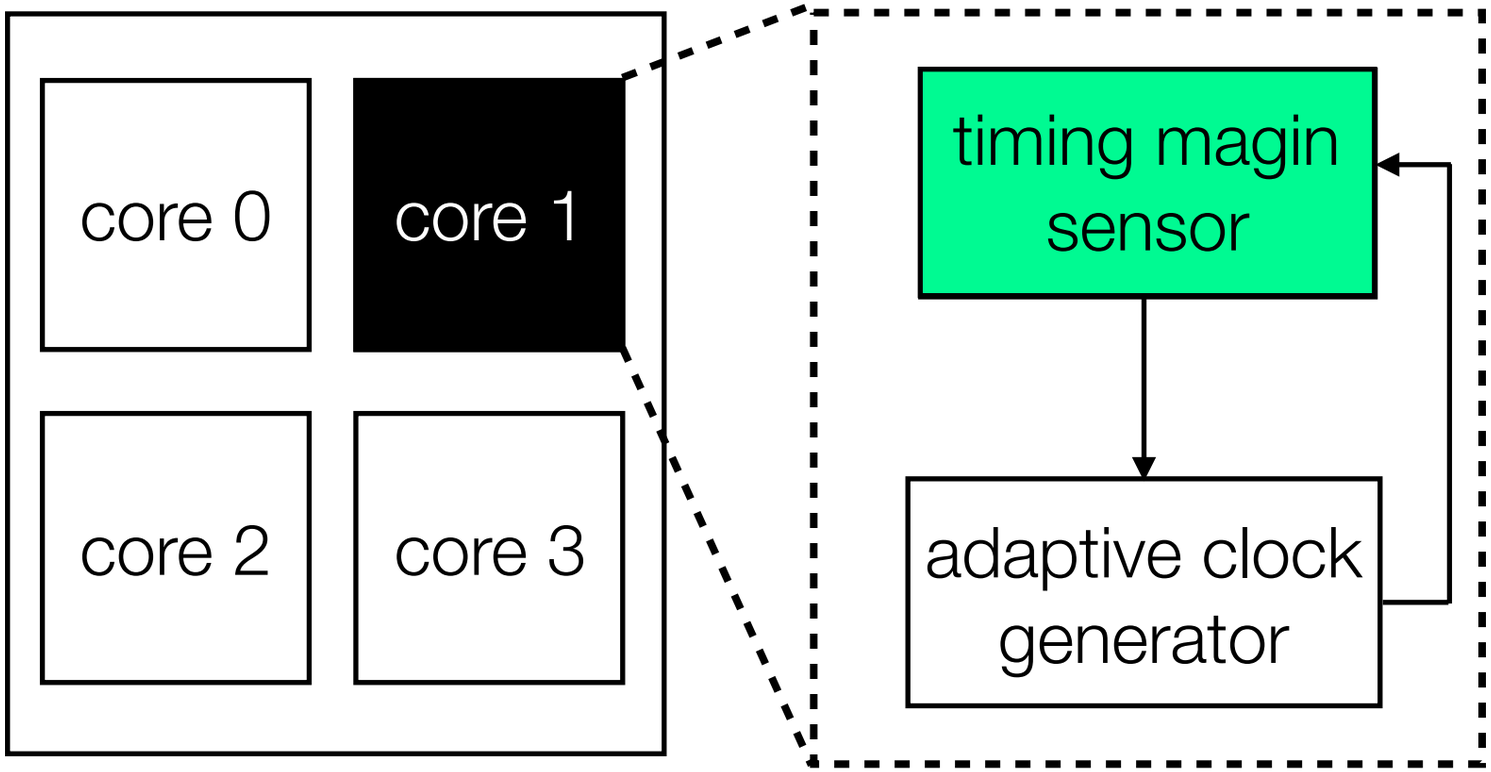

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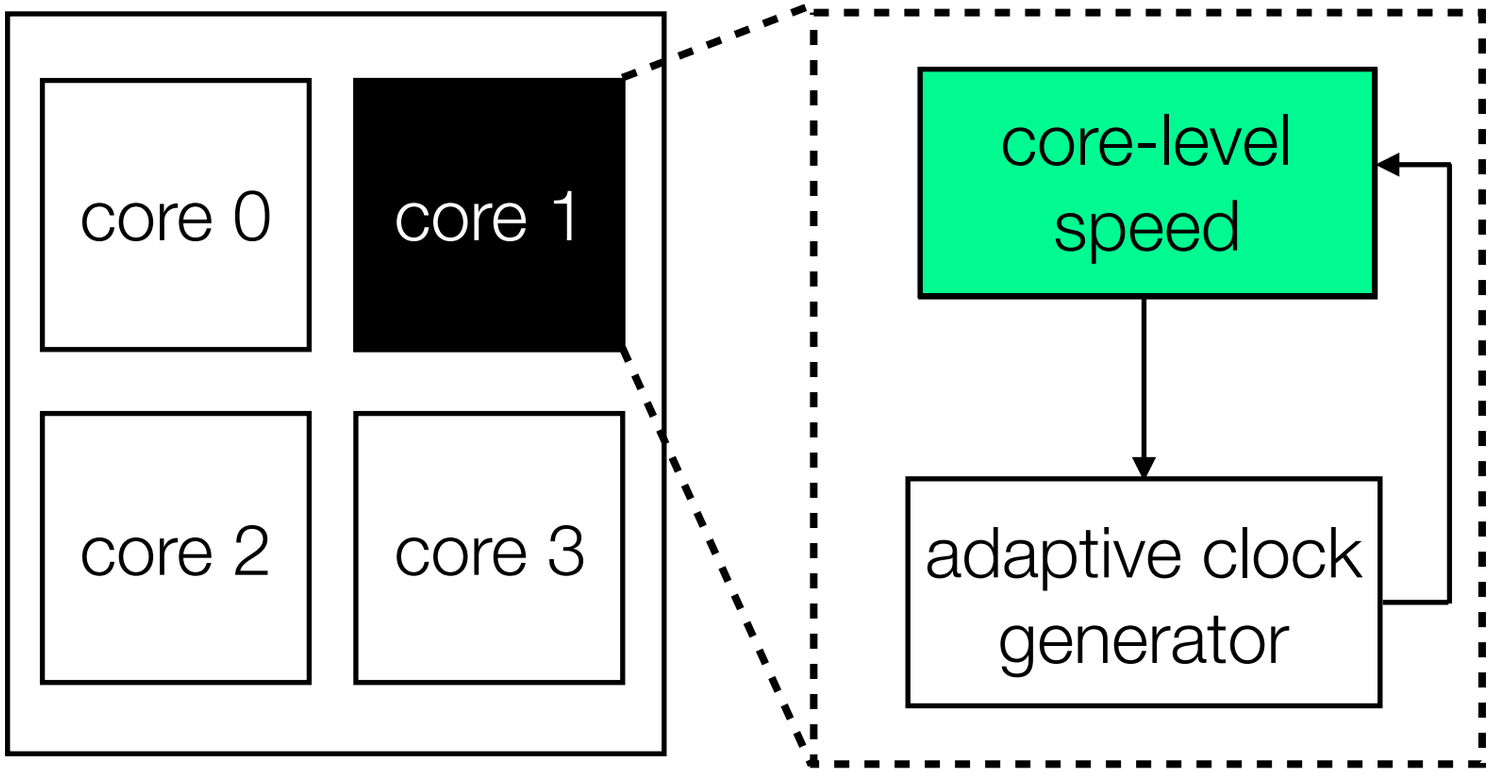

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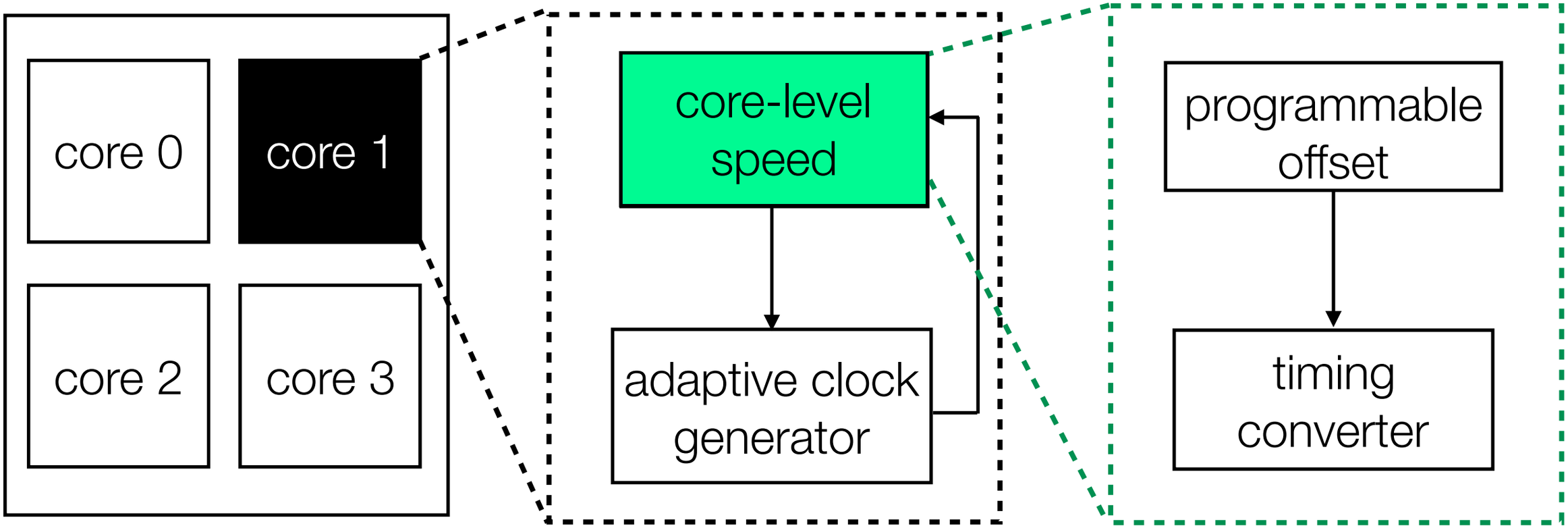

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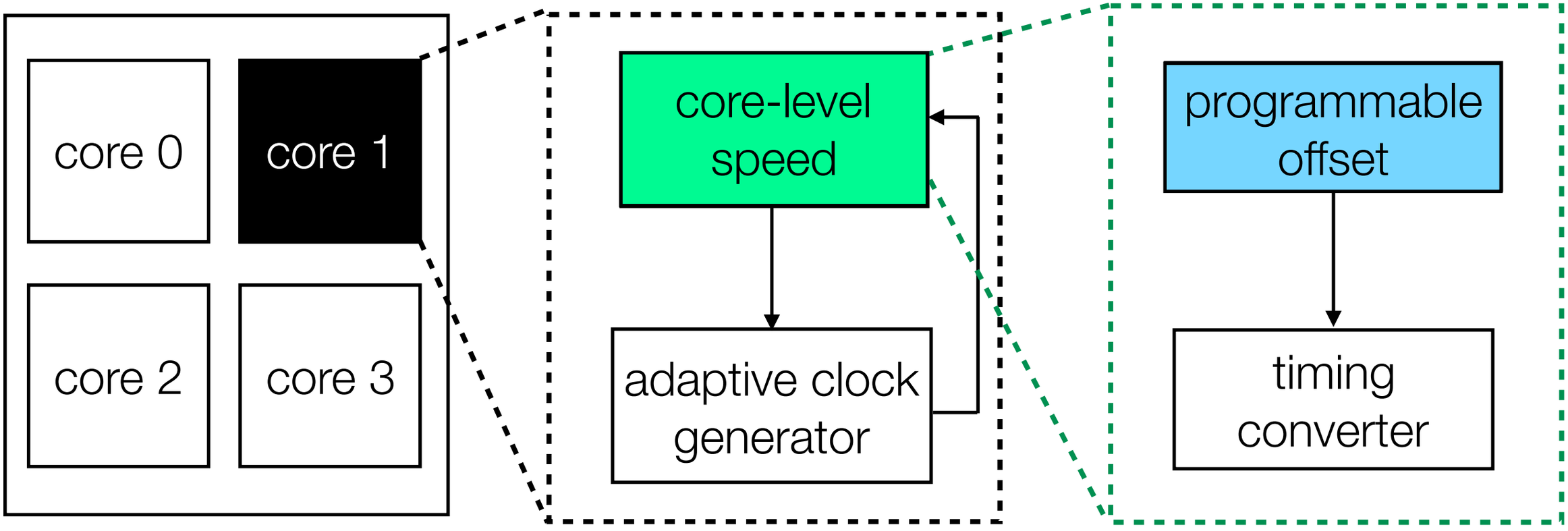
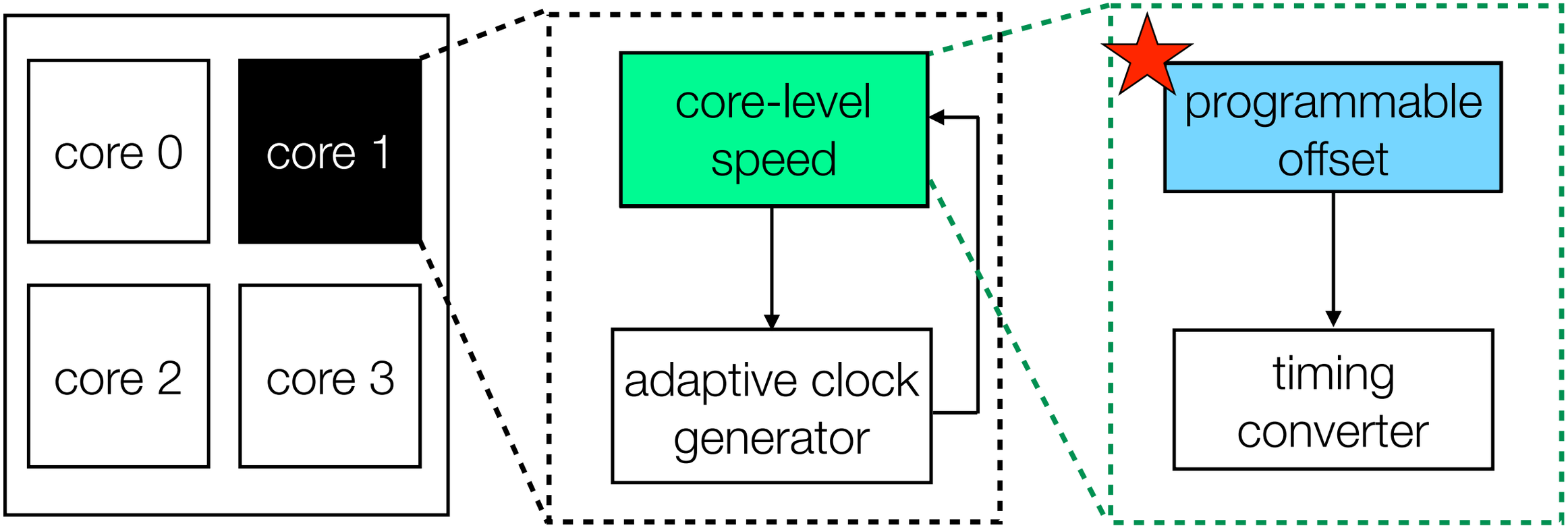
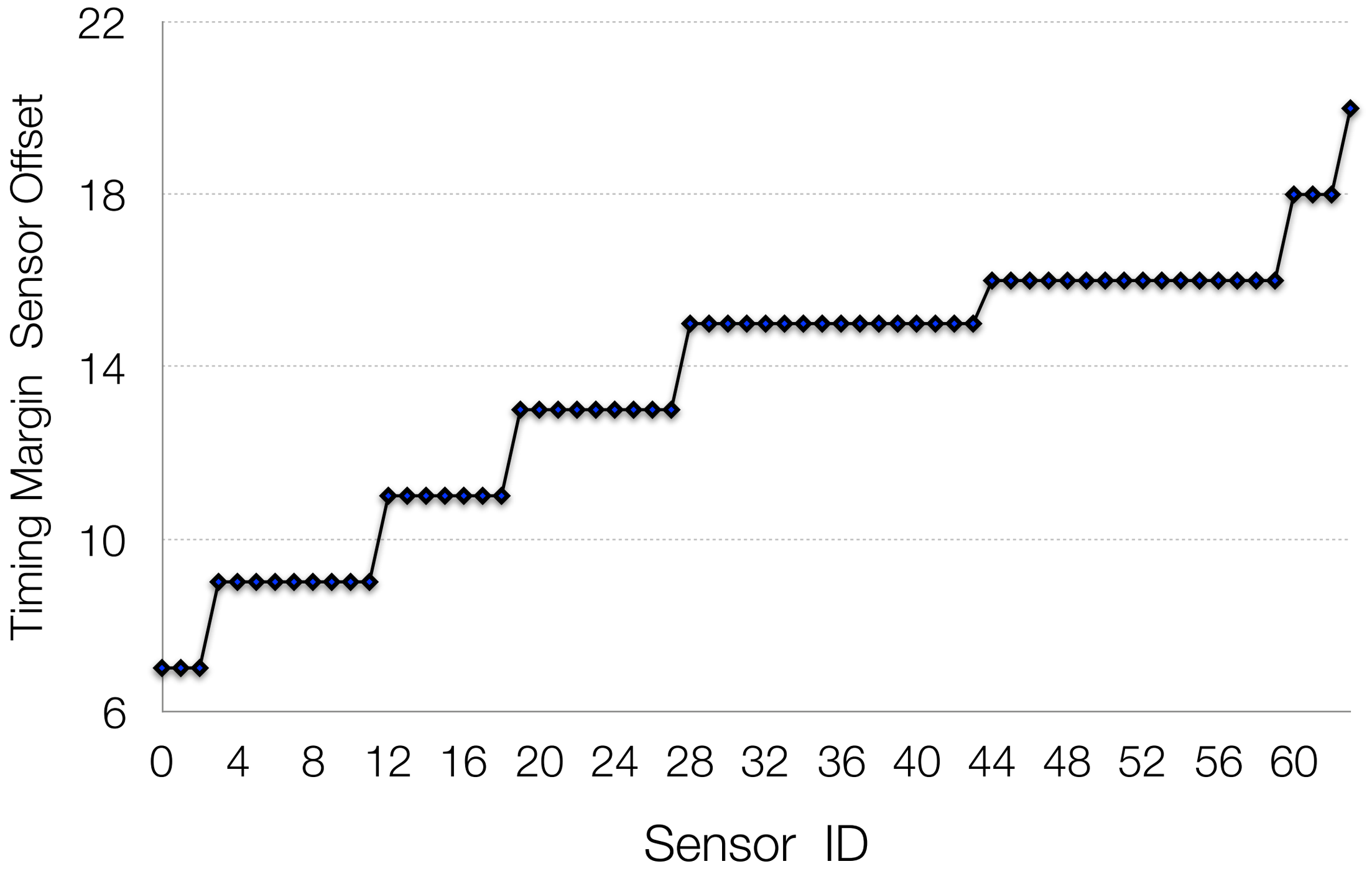


Expose Core-level Performance with ATM

preset measurement offset
to hide process variation



Preset Timing Margin Measurement Offset



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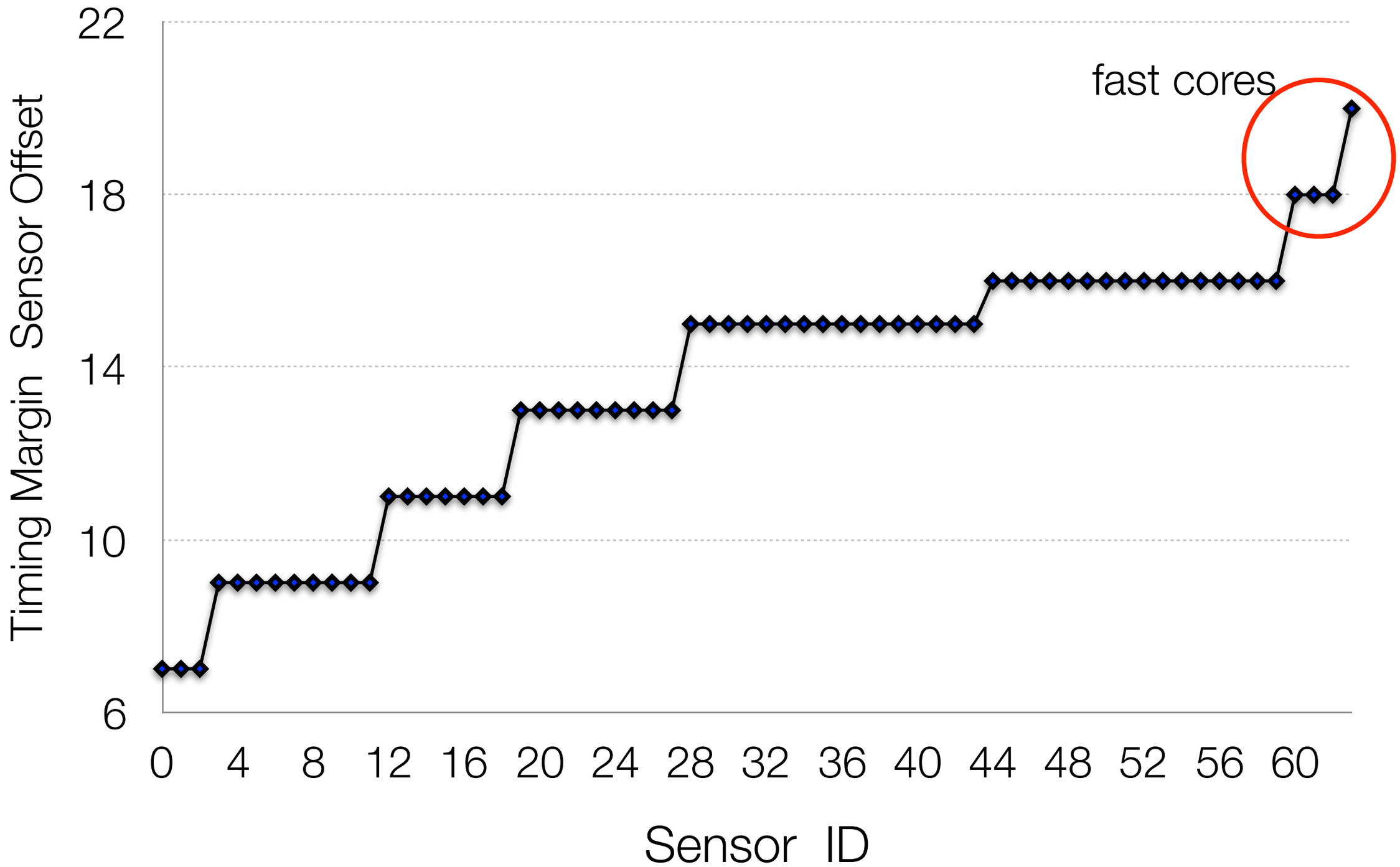

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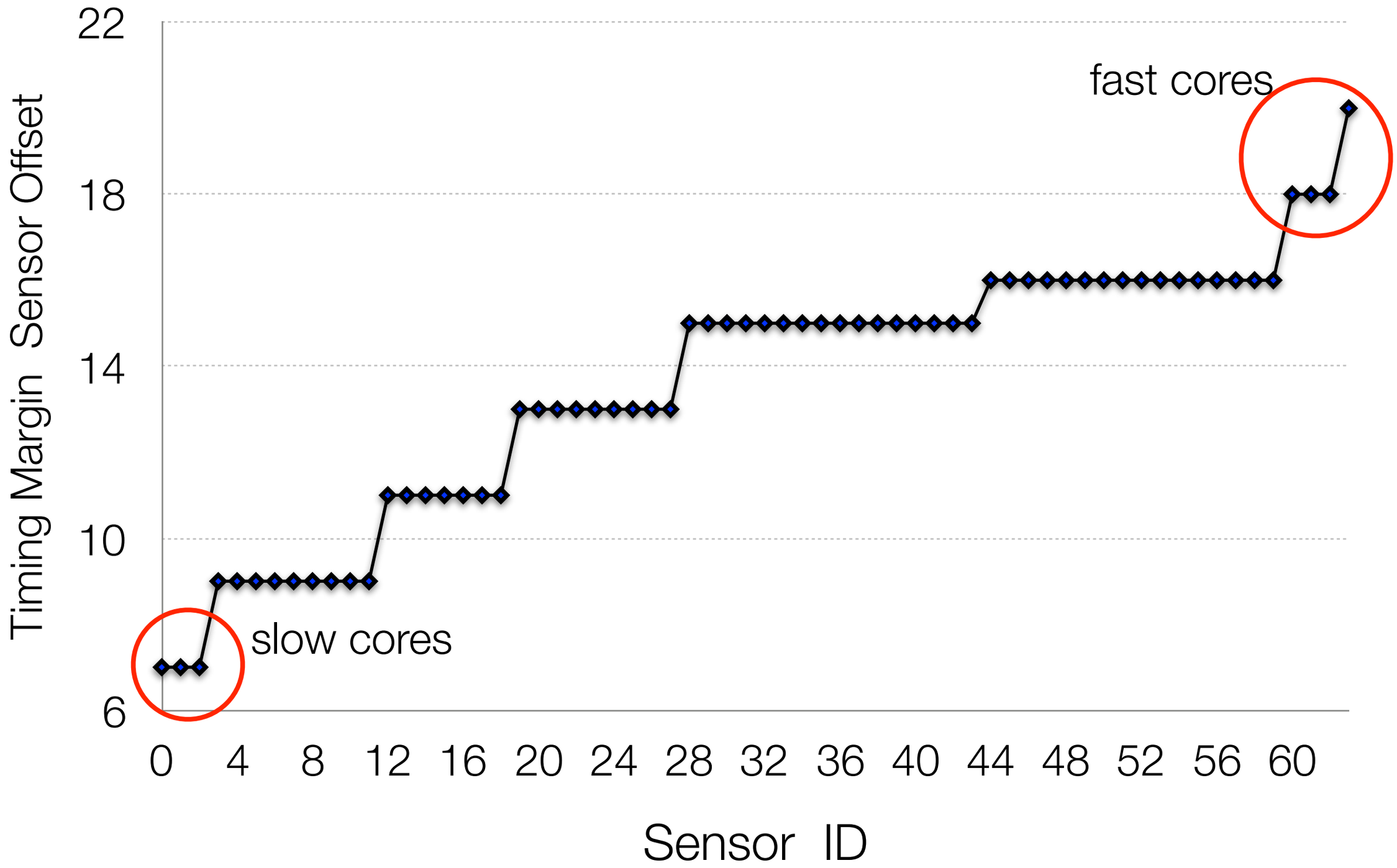

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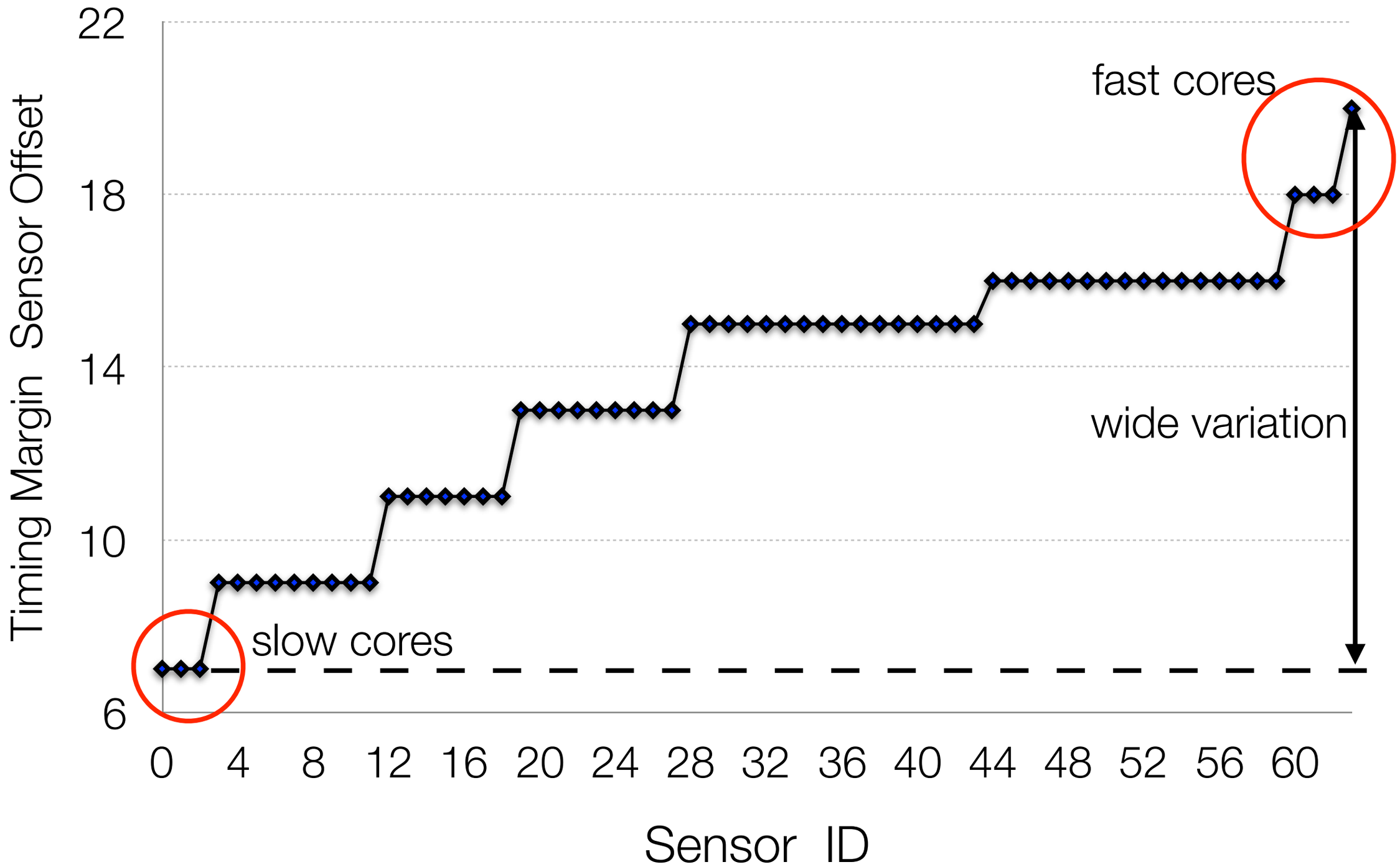

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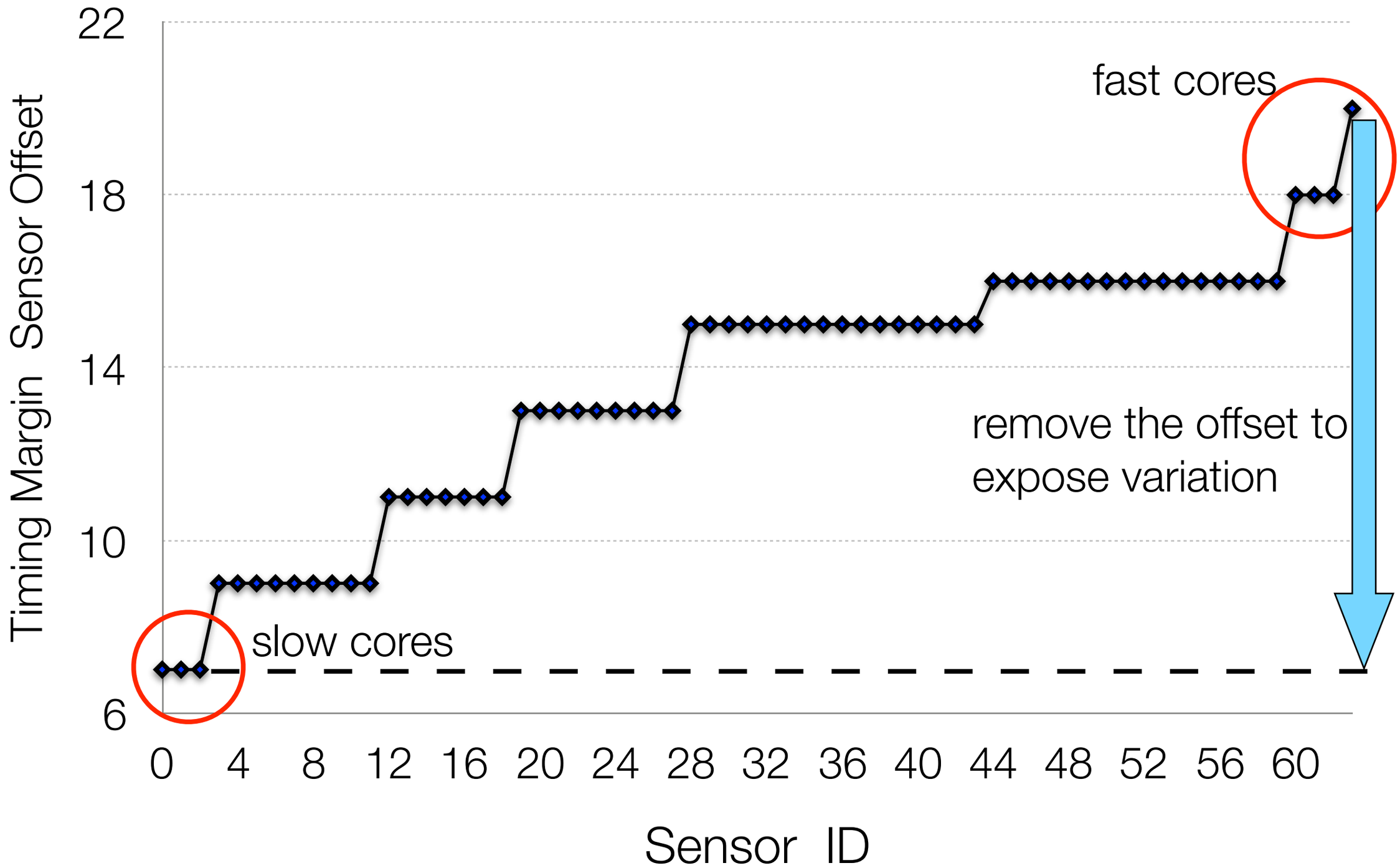
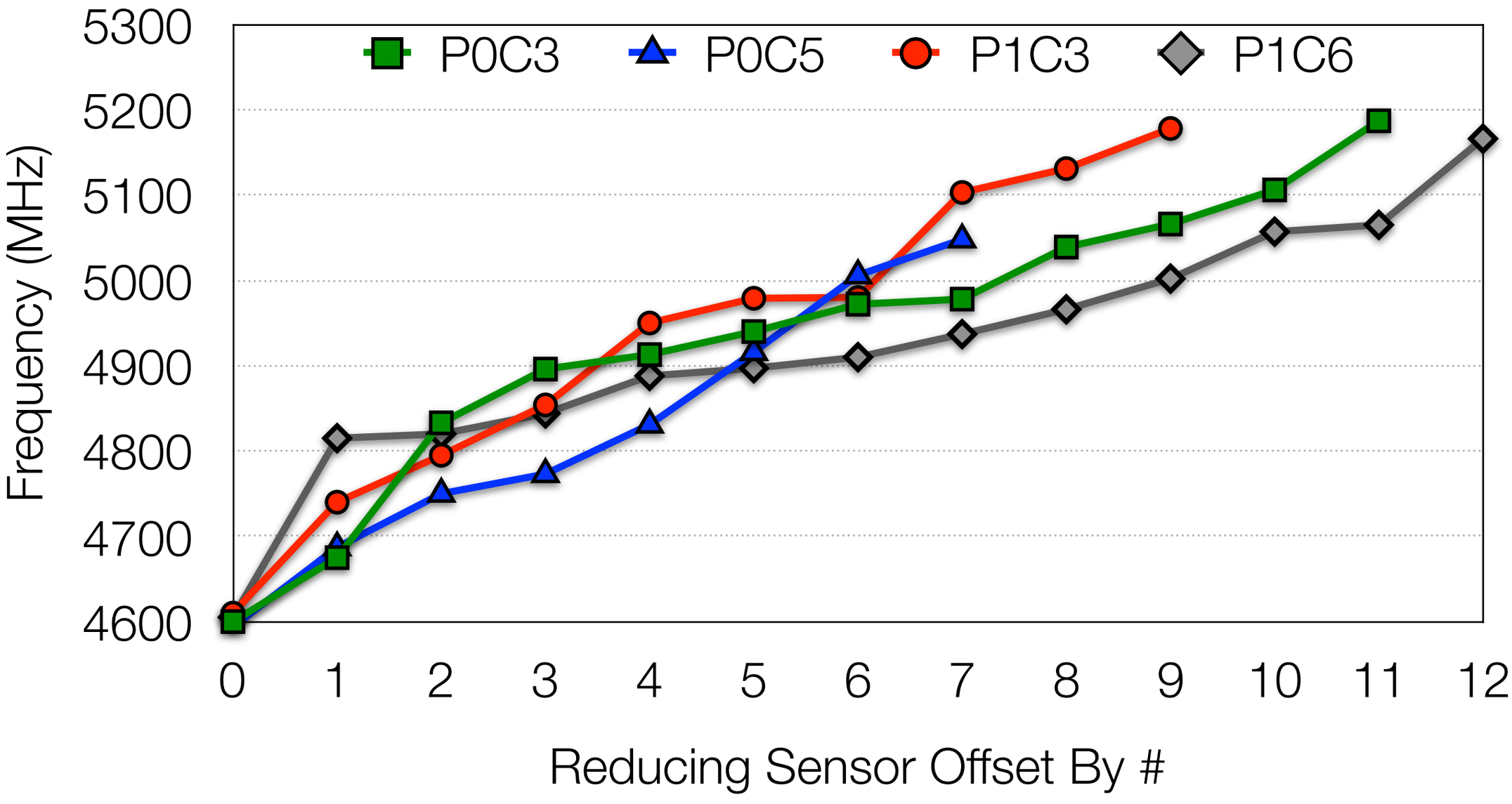


Re-Program Timing Margin Sensor to Fine-tune Core-level Performance



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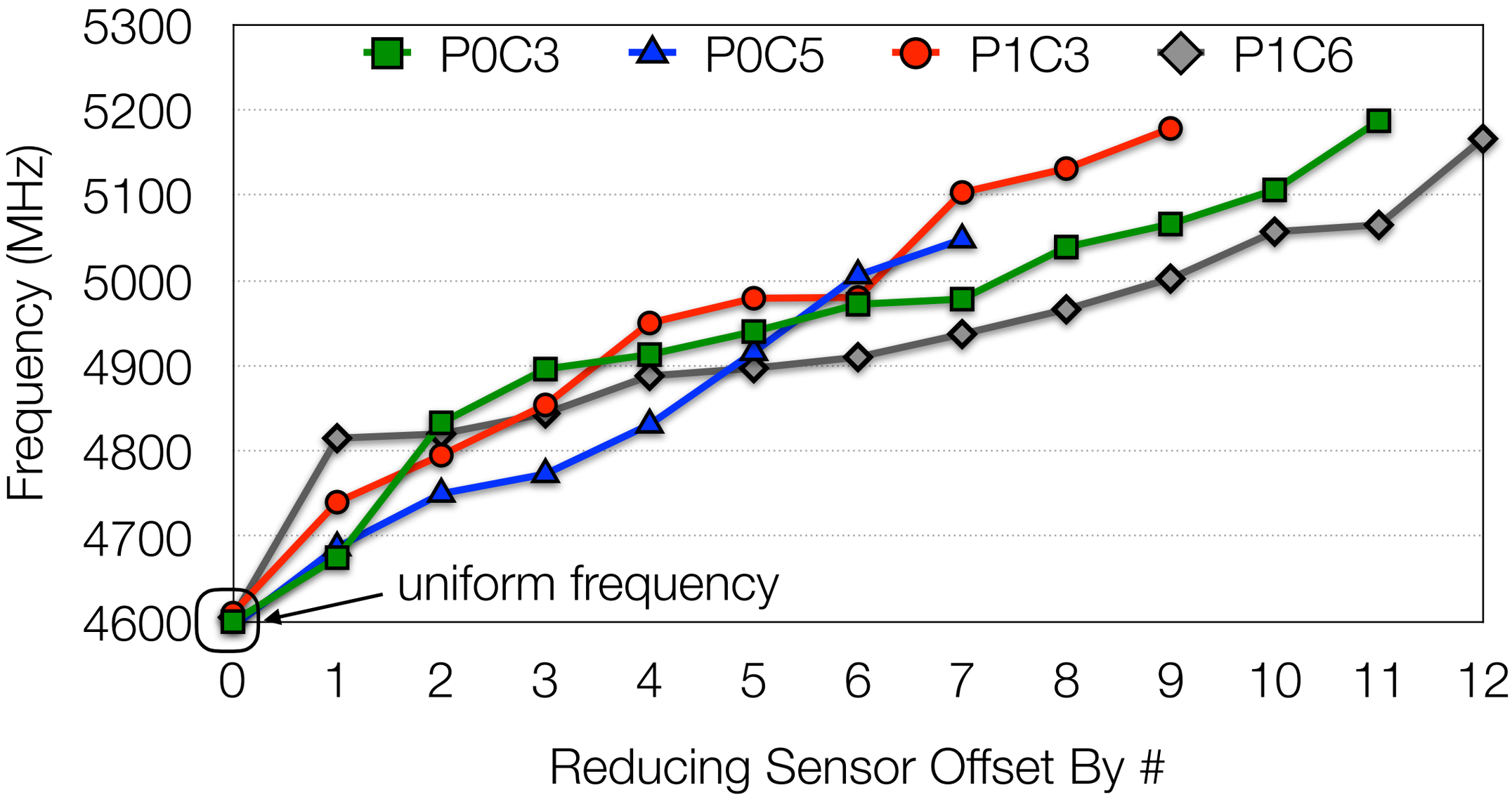

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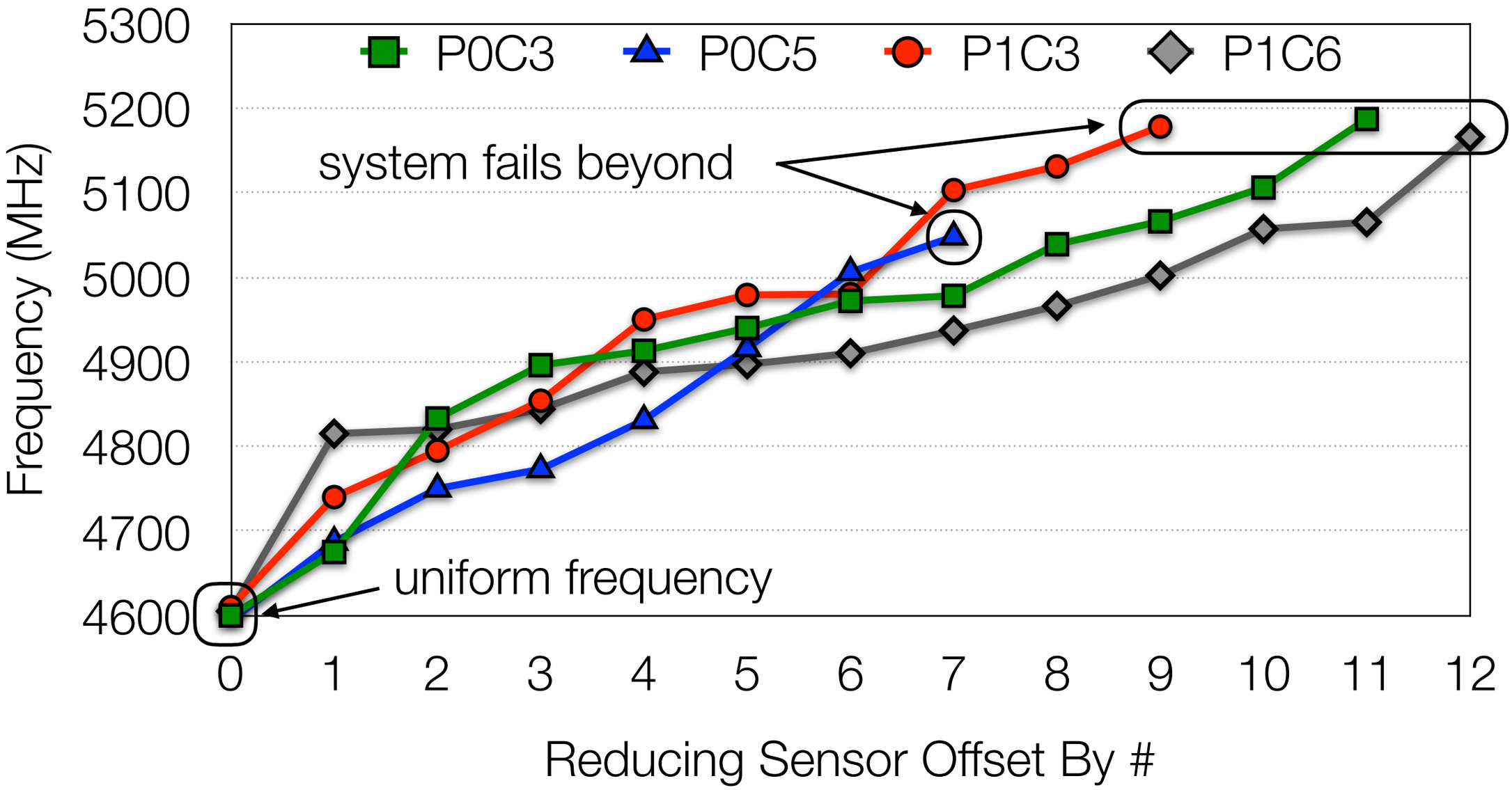
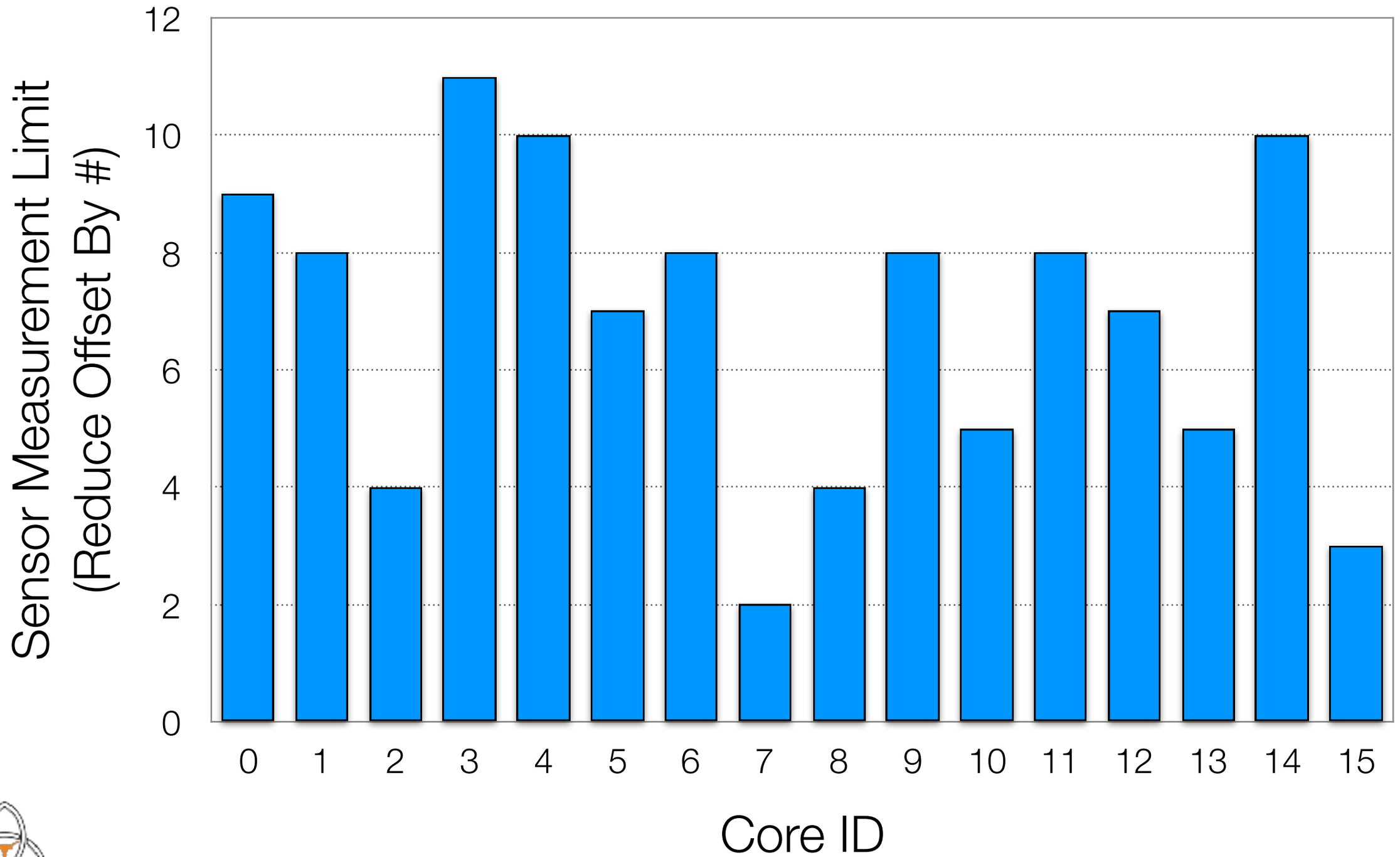


Core-to-core Sensor Configuration variation



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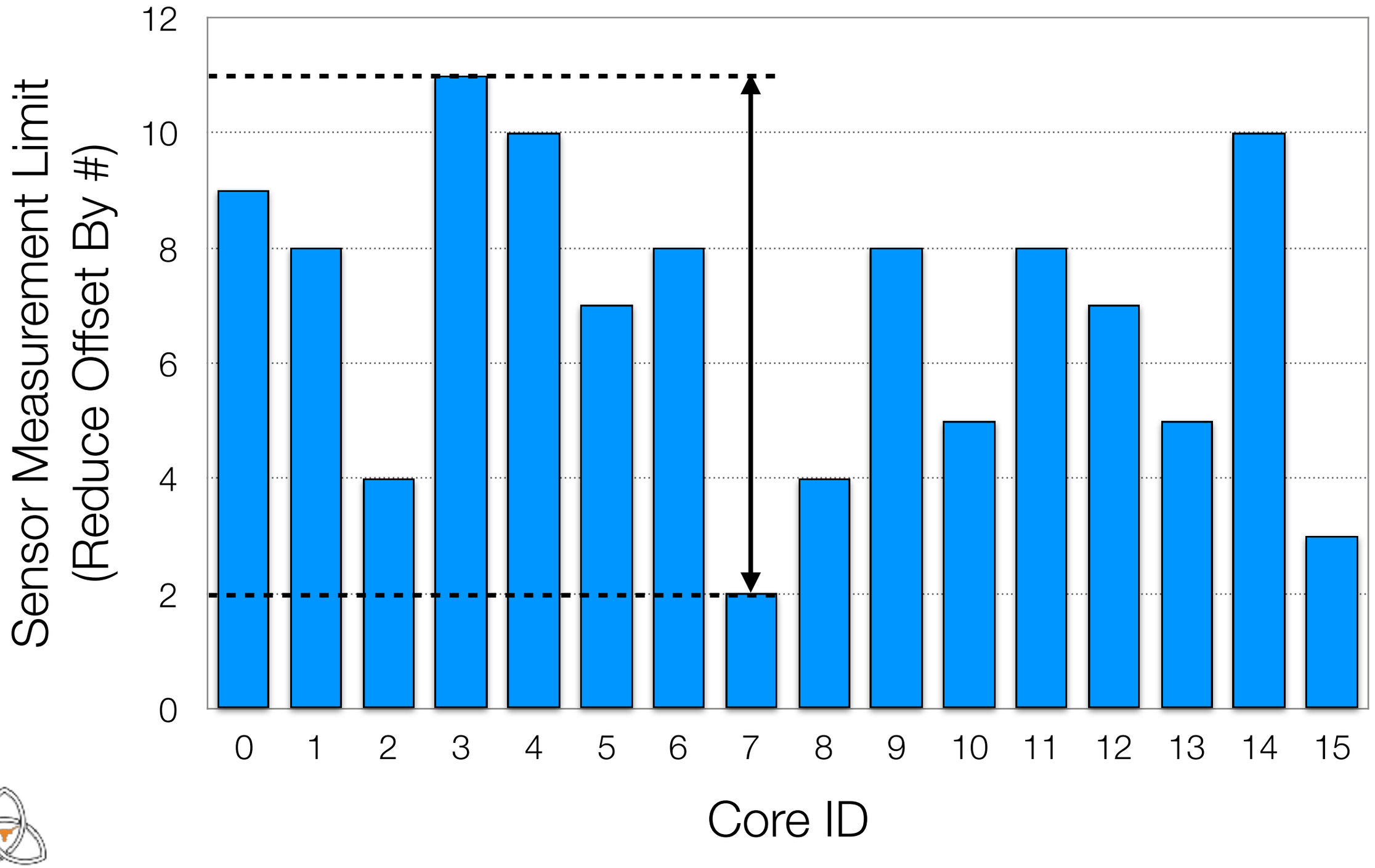
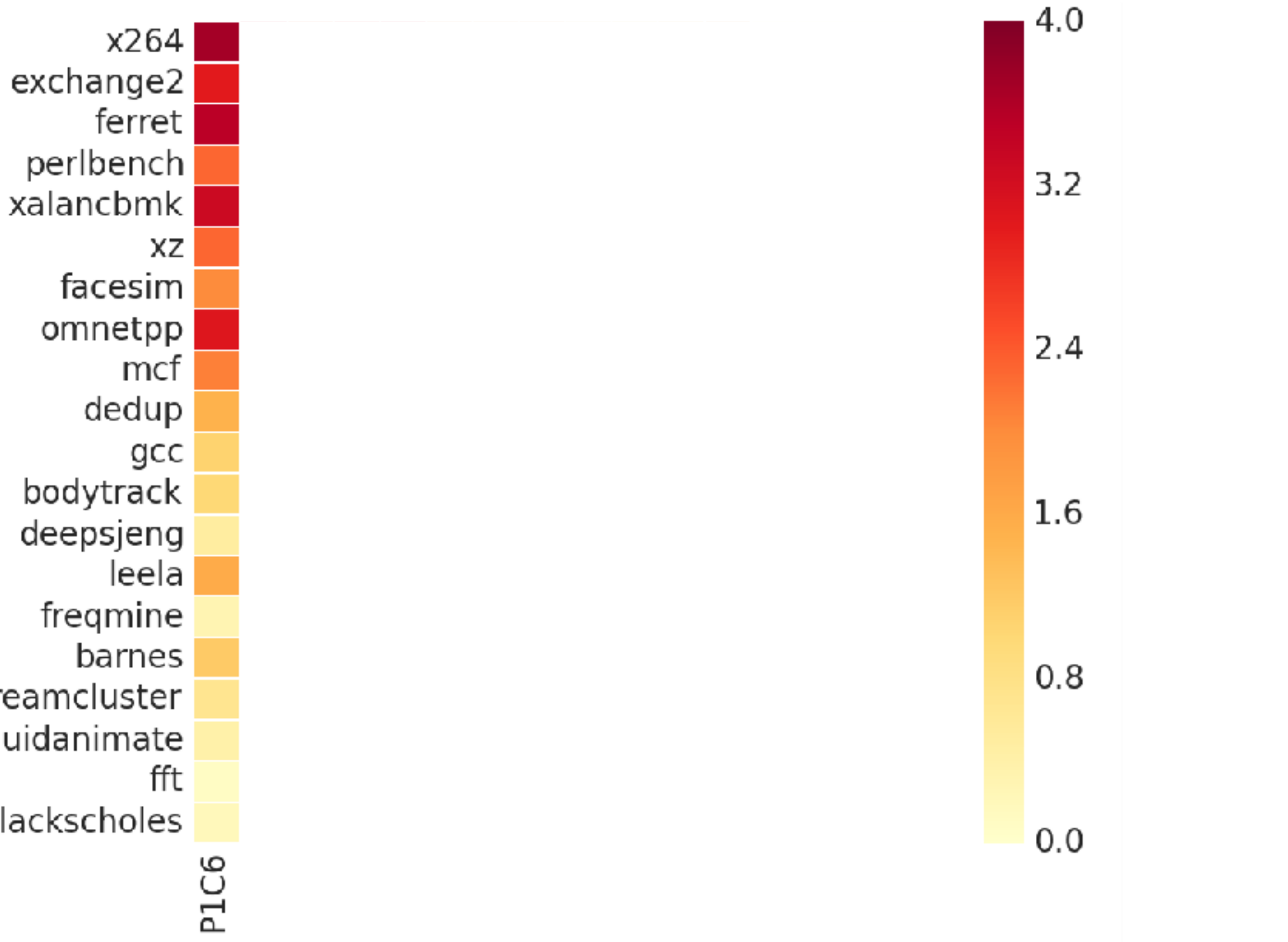


Running applications: Rollback from System Idle Limits



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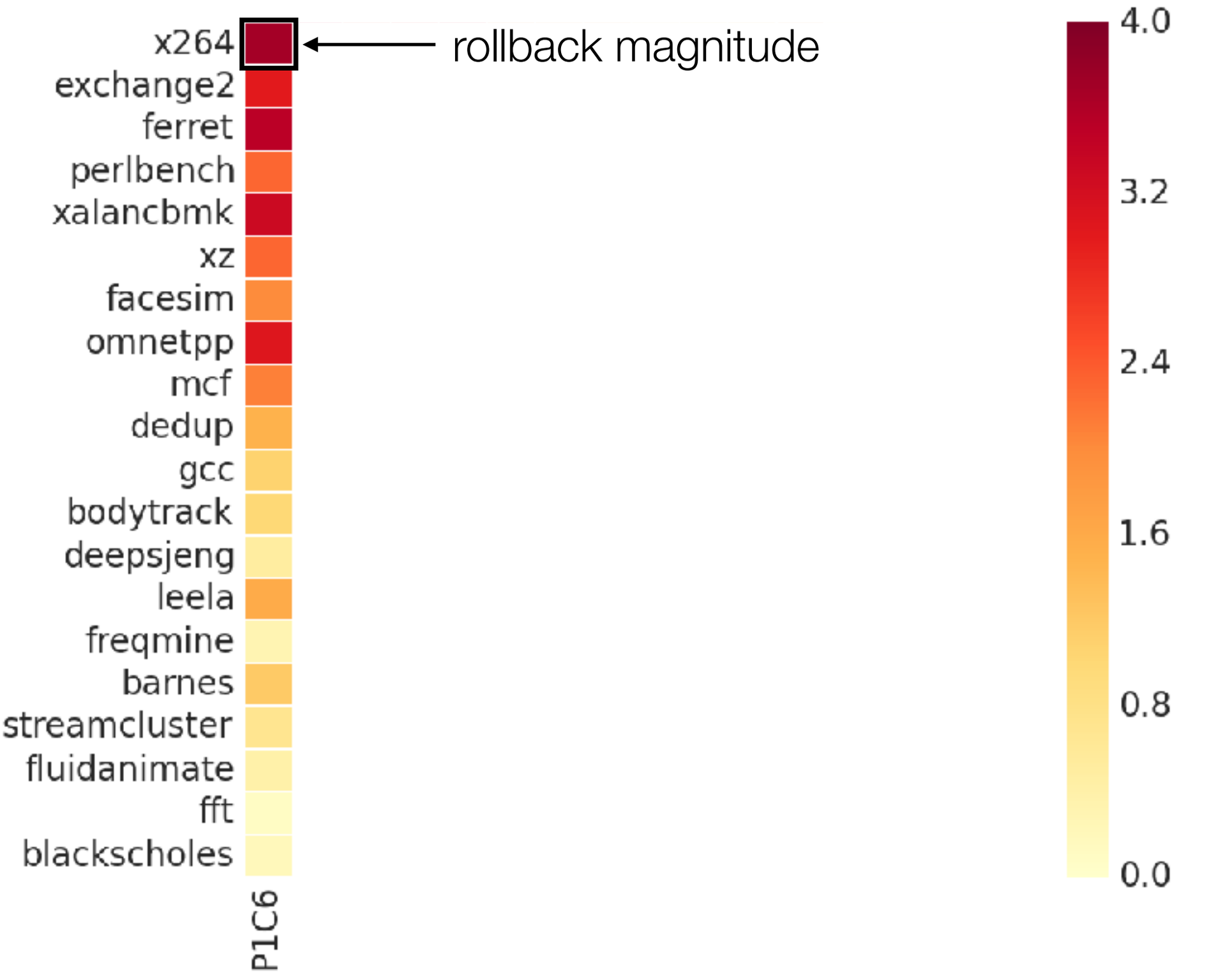

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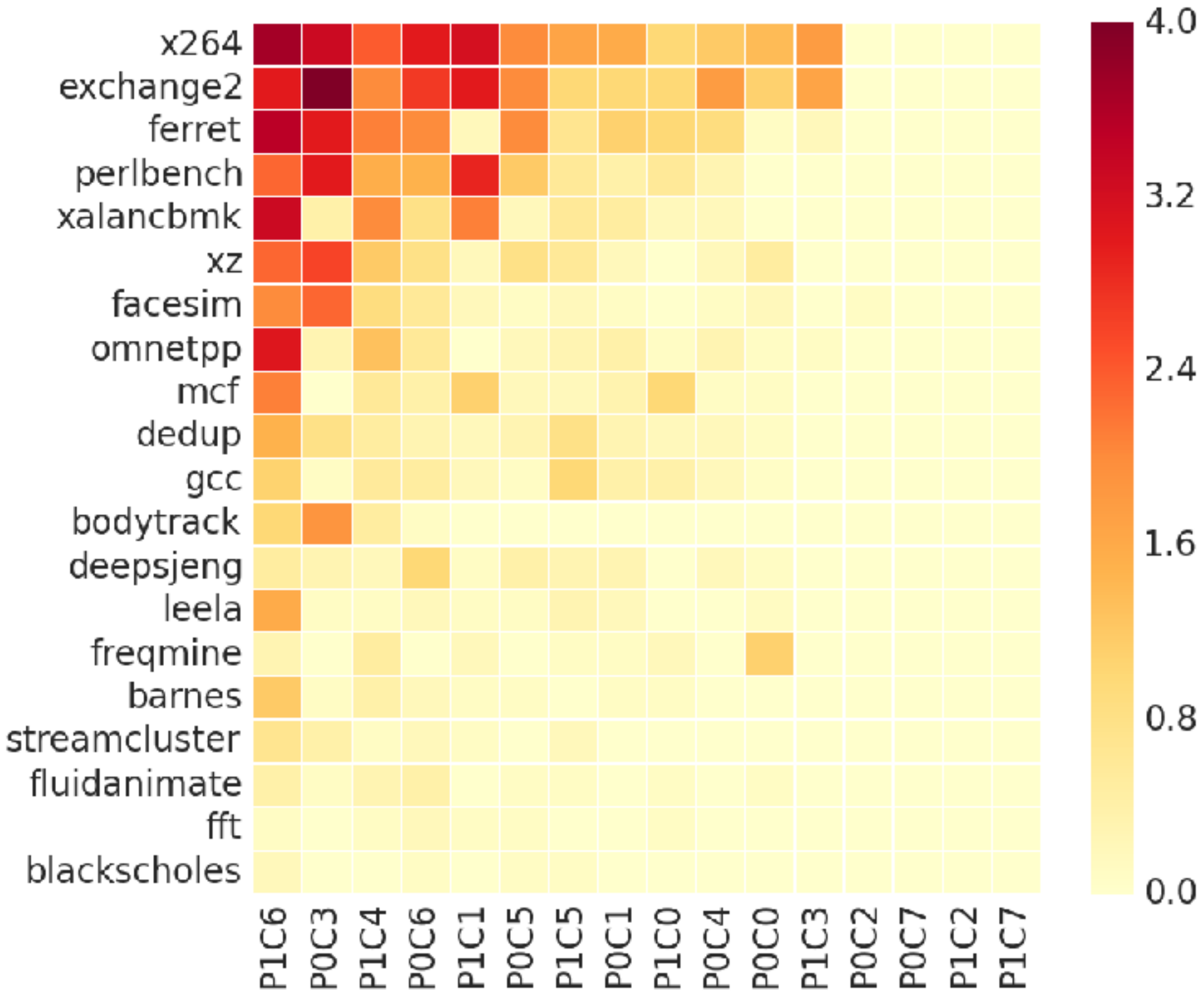

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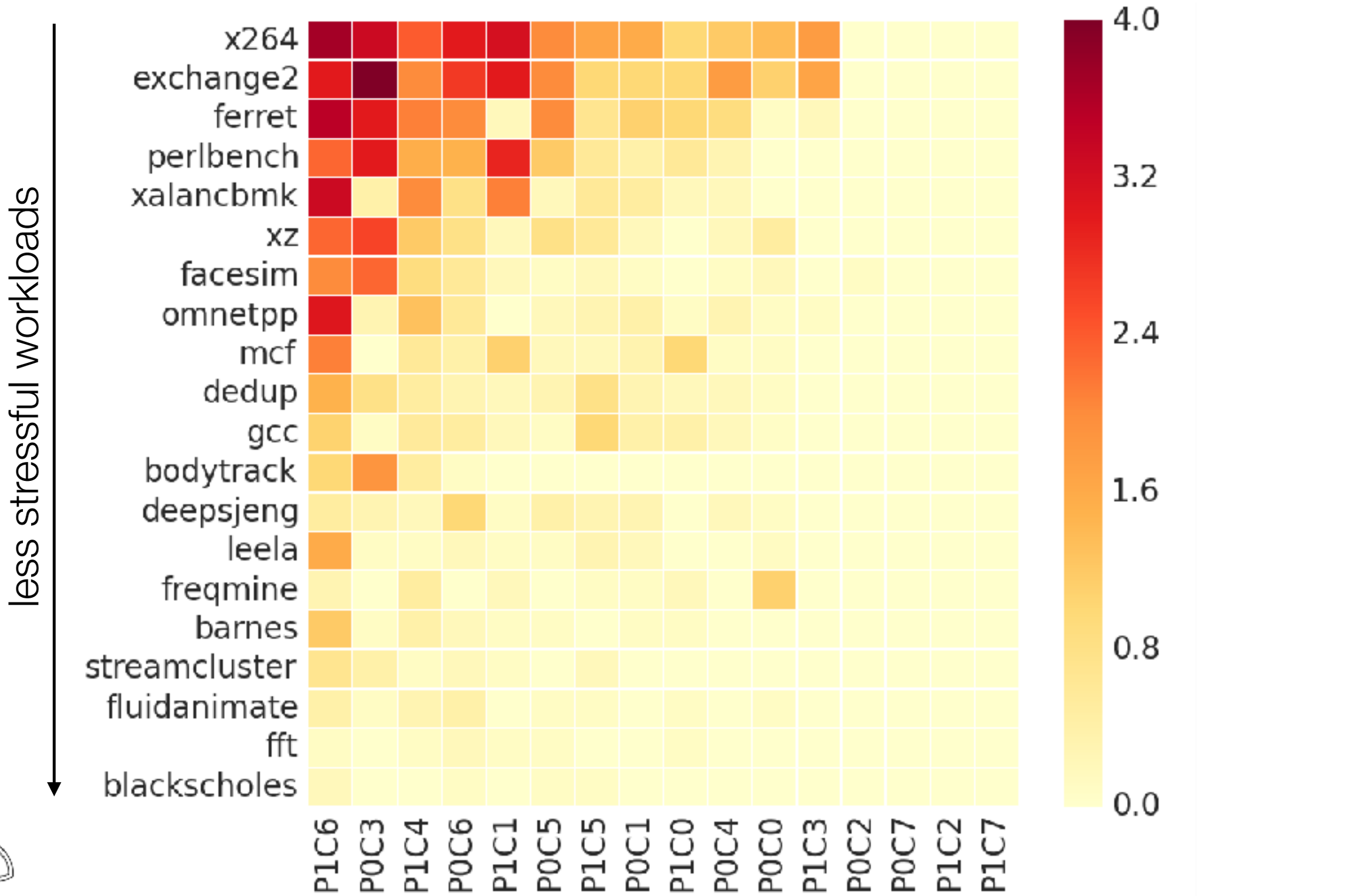

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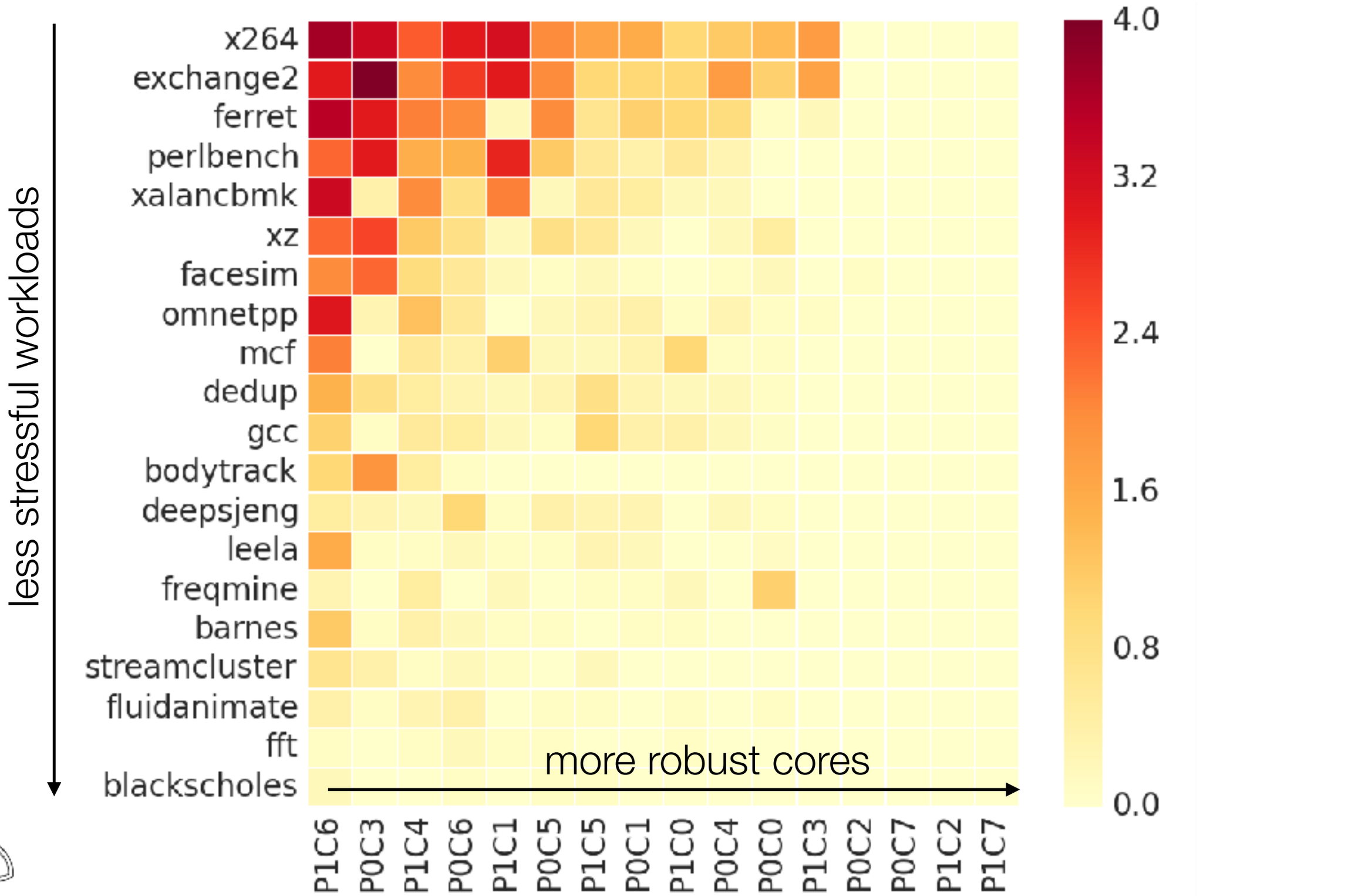

Fine-tuning Active Timing Margin

- Option 1: predict ATM config for each <App, Core>

	Evaluation	Reason
complexity		
improvemnt		

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	Evaluation	Reason
complexity	high	
improvemnt		

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	Evaluation	Reason
complexity	high	di/dt effect, input data, instruction coverage, etc.
improvemnt		

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improvemnt	low	

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	Evaluation	Reason
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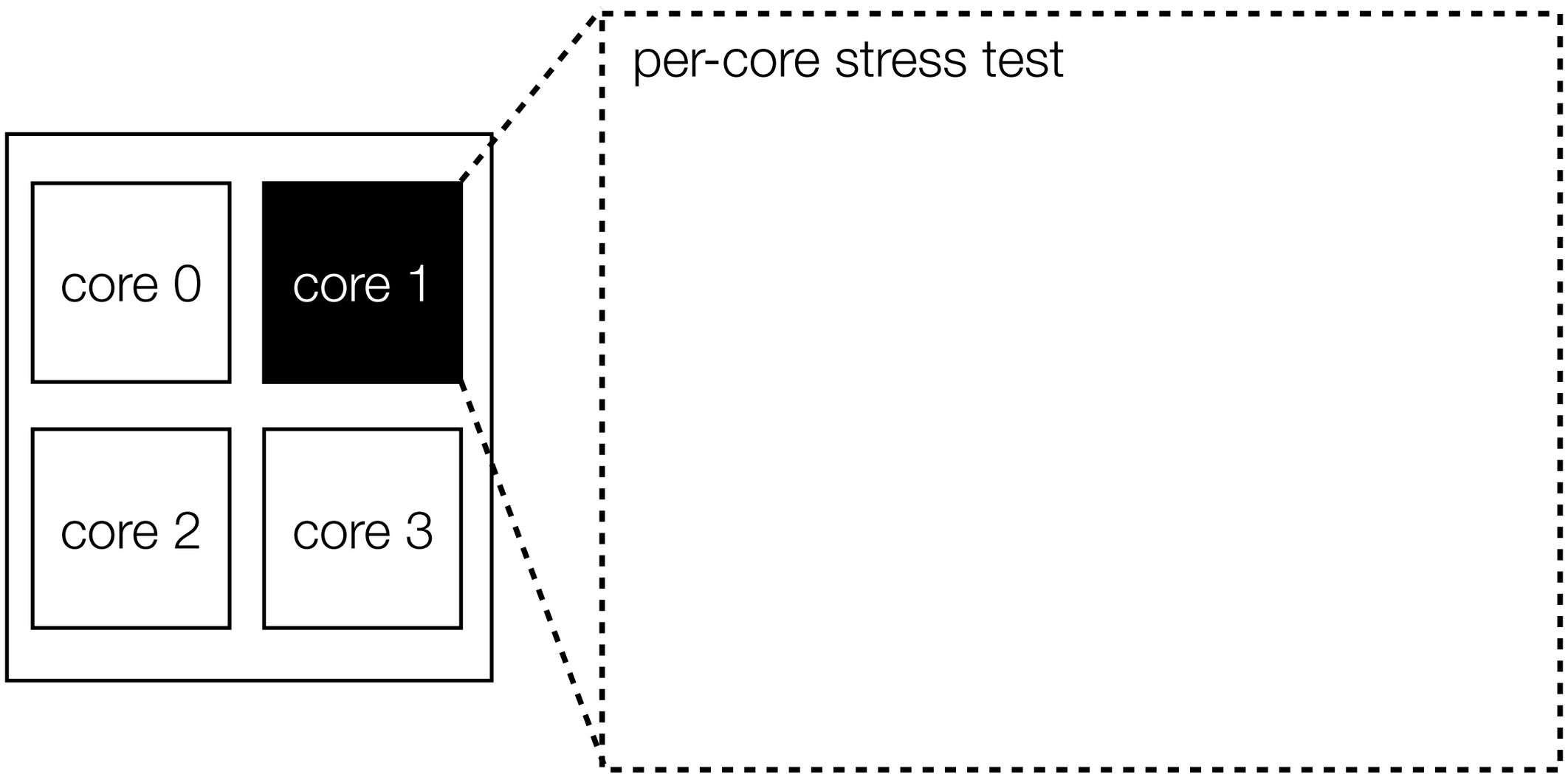
✓ Option 2: apply one configuration for all apps

Fine-tuning at Test-time

- Set timing margin sensor offset with core-level stress test



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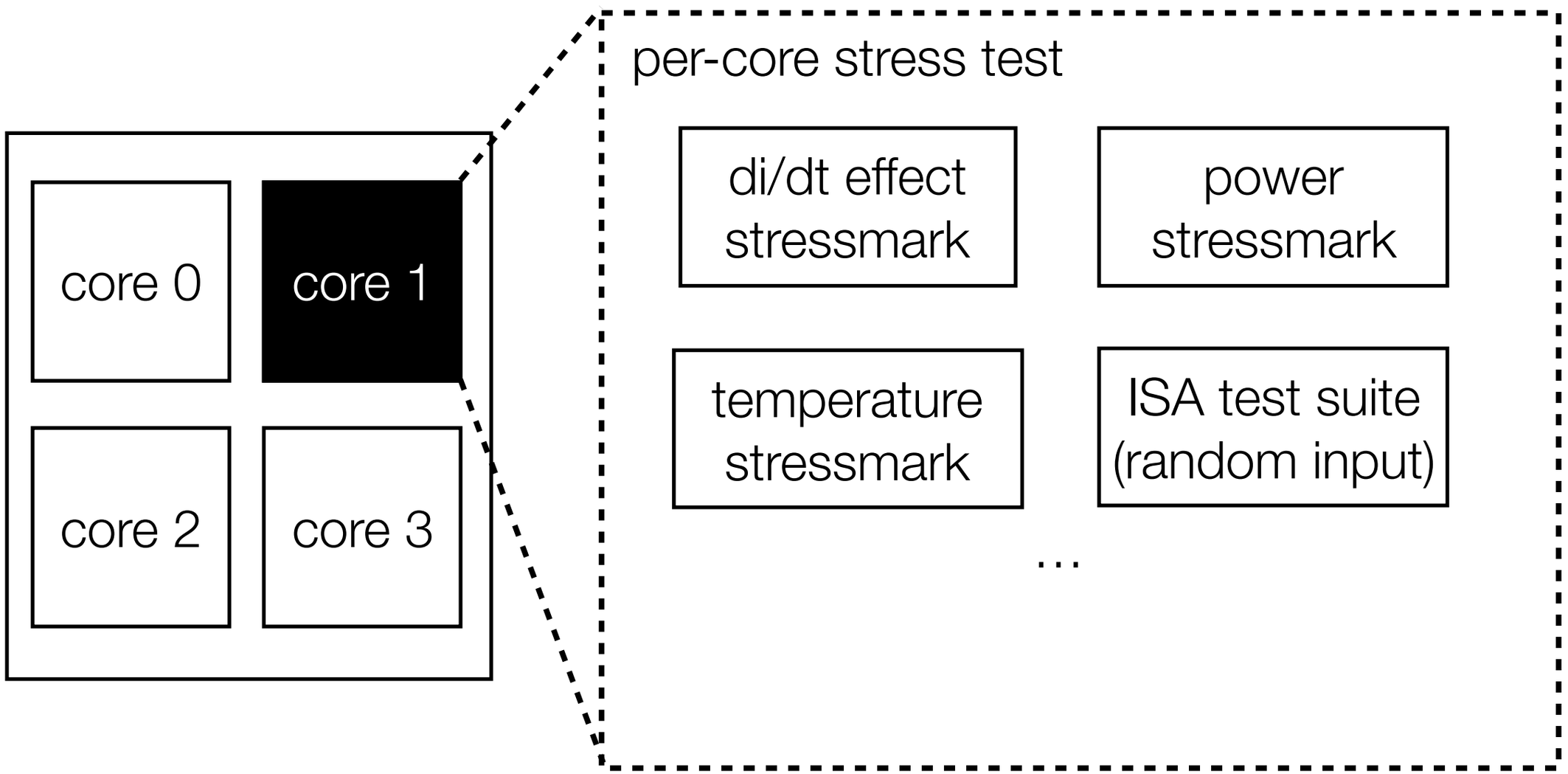

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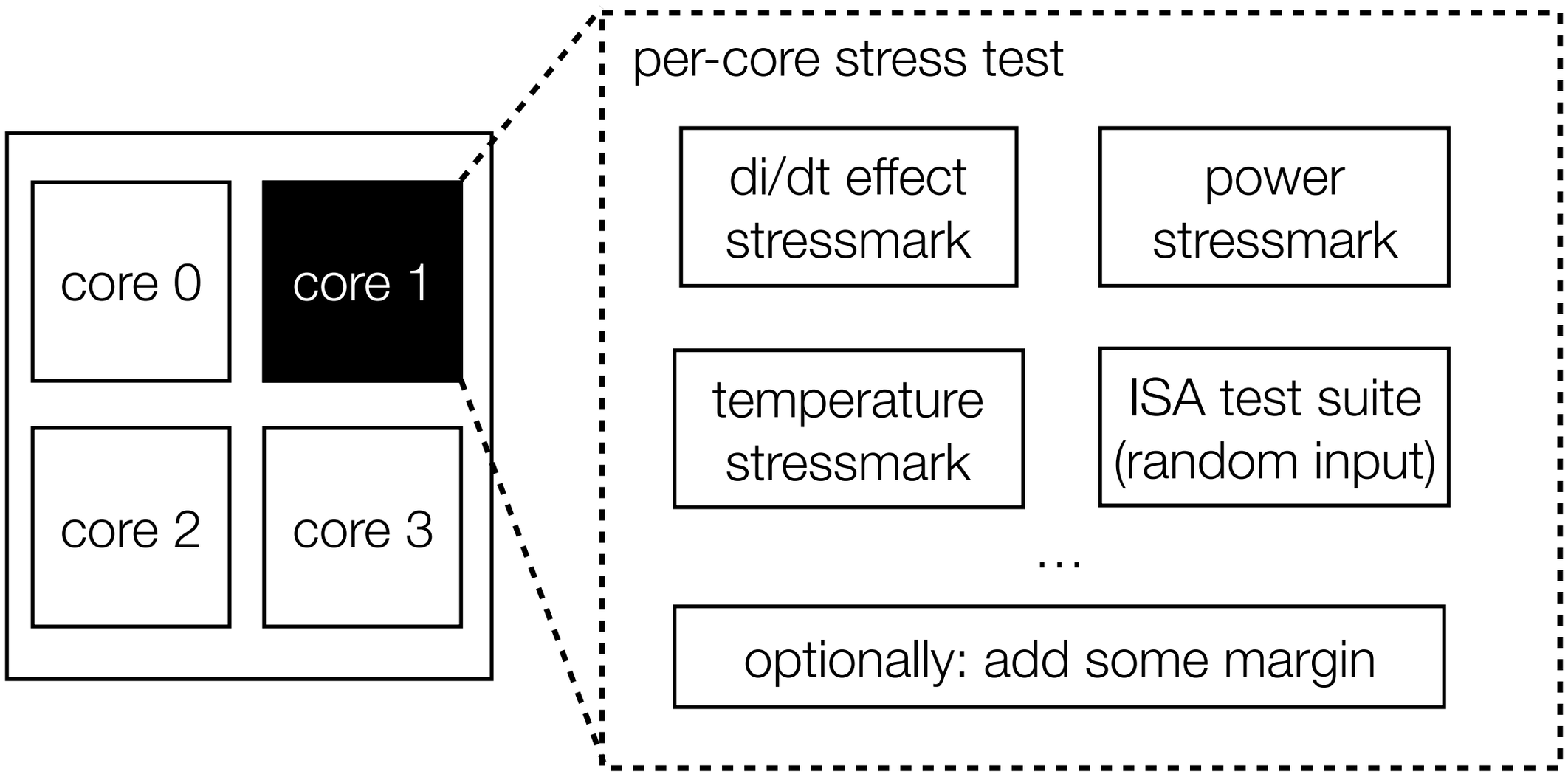
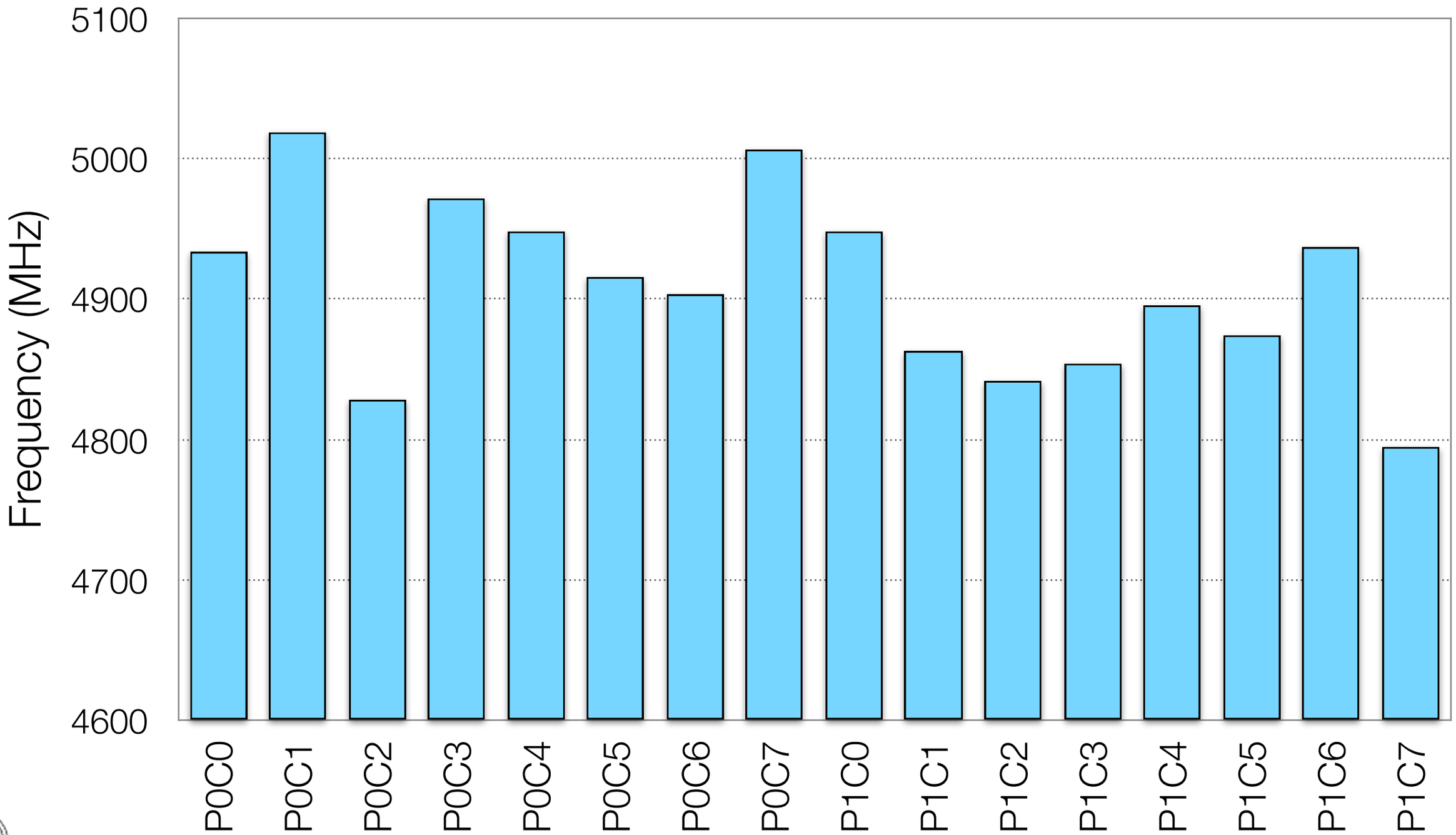


Fine-tuning ATM to Expose Variation



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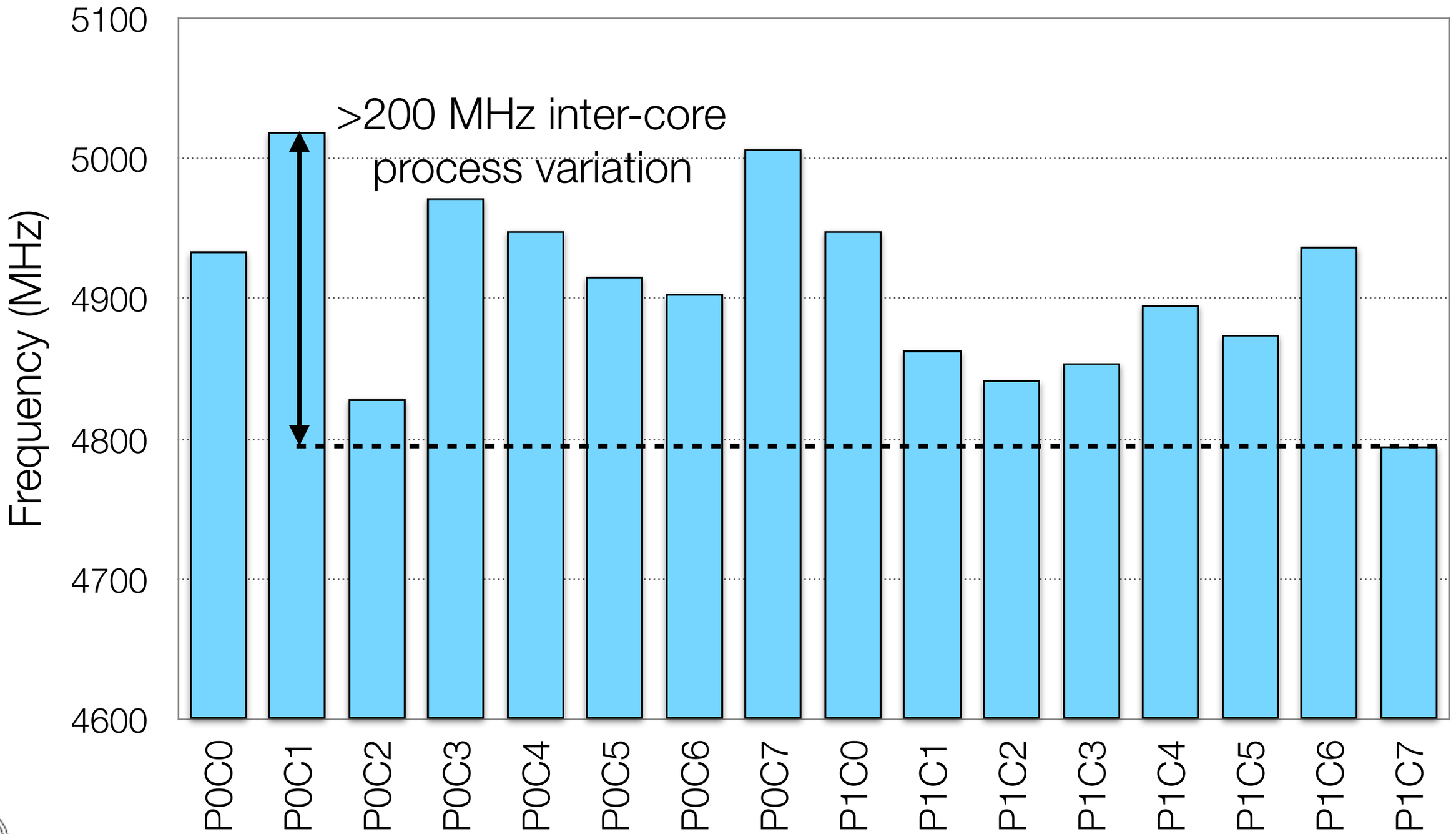

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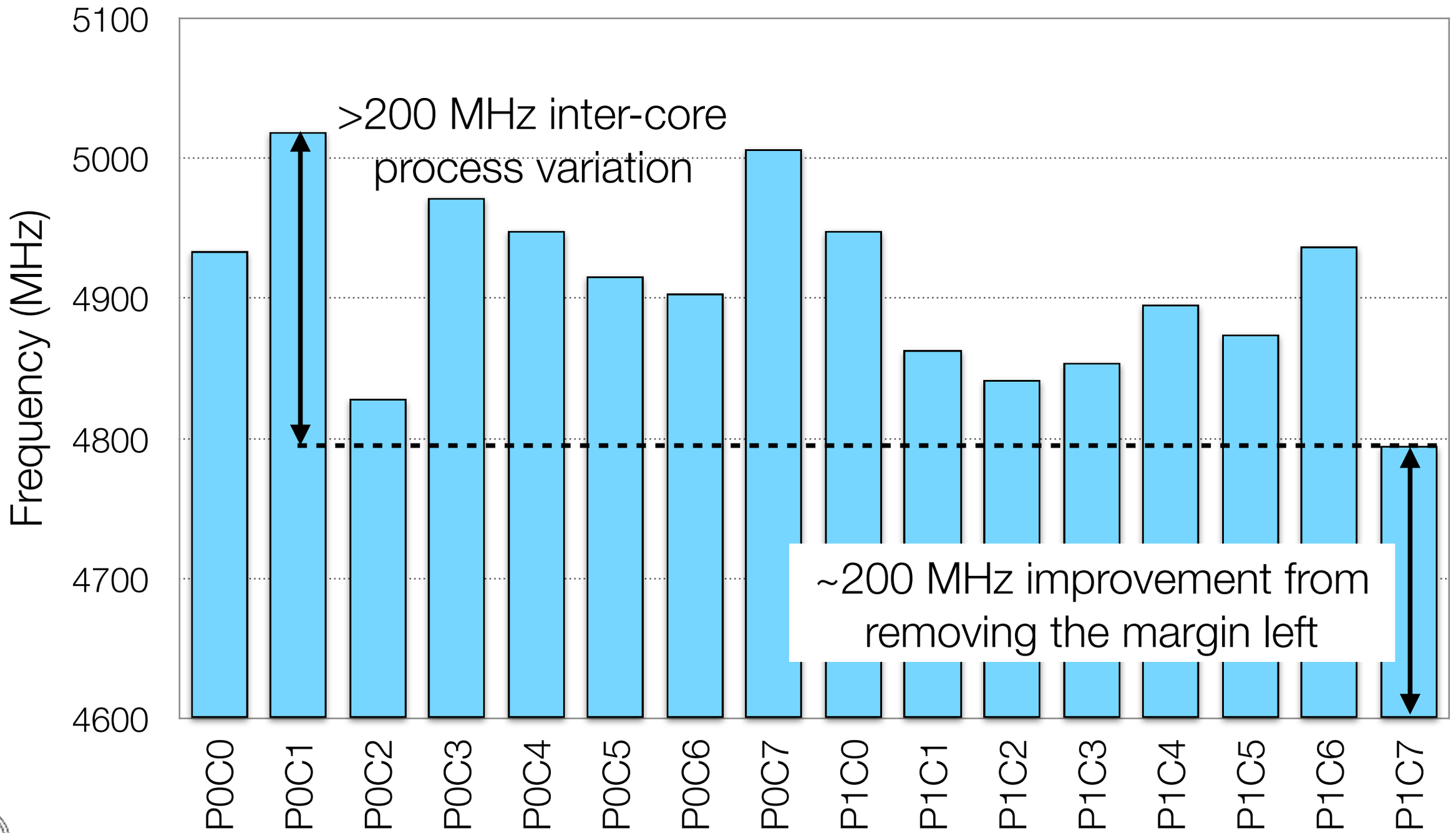
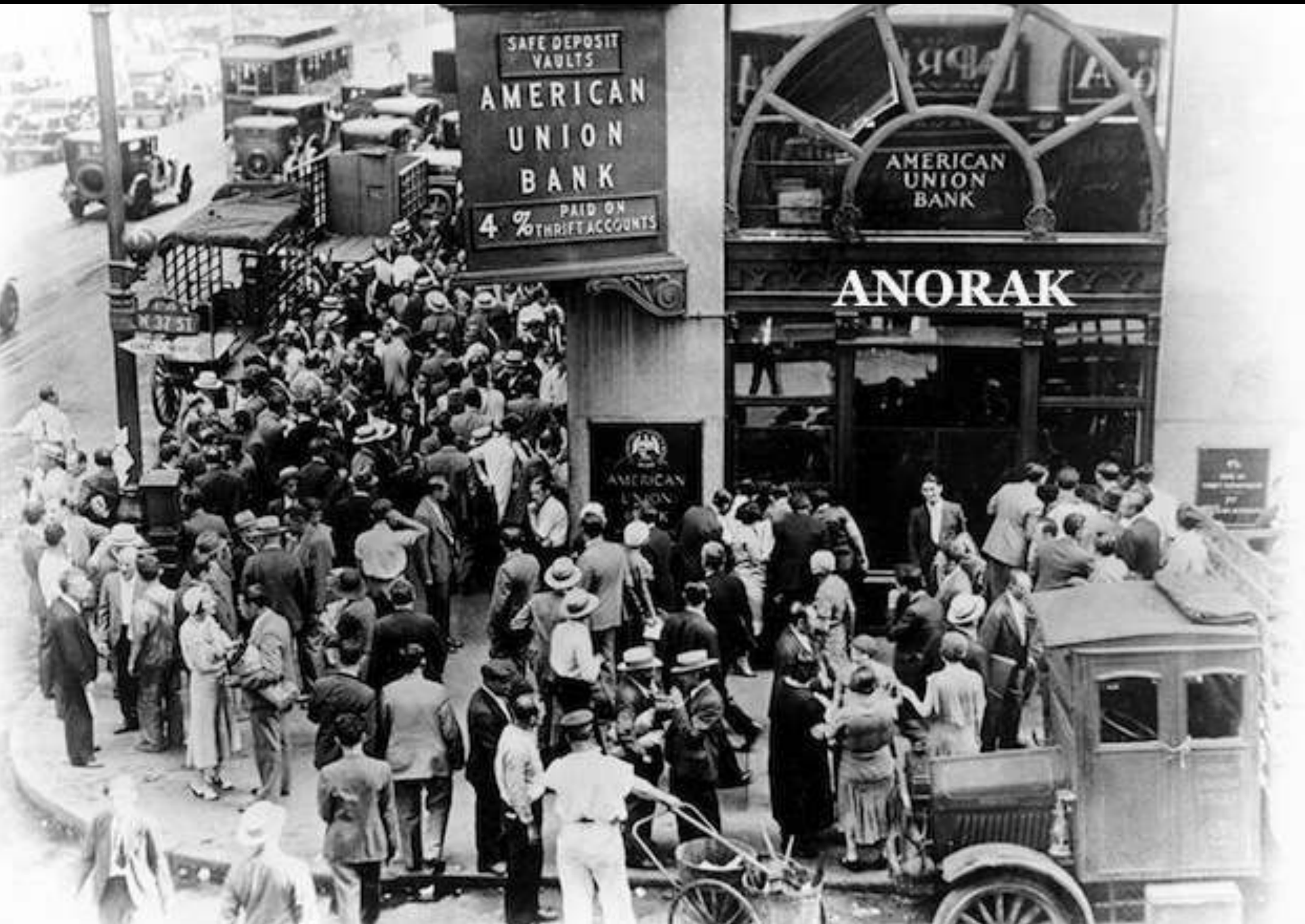


“Bank Run” on Active Timing Margin

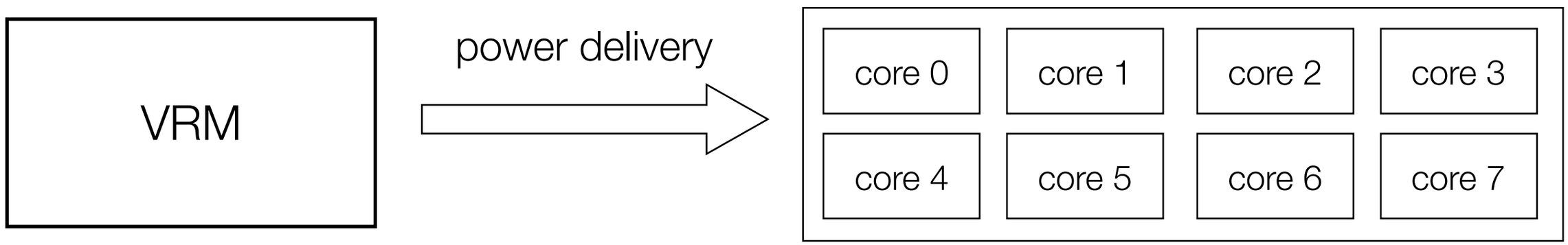


Executive Summary

- Fine-tune core-level ATM to **automatically** expose inter-core performance variation

- Expose chip-wide performance variation caused by heterogenous workload intensity

“Bank Run” on Active Timing Margin



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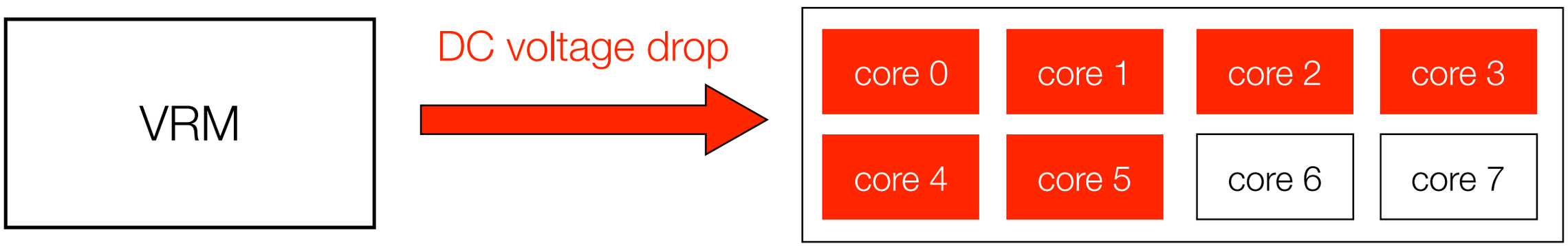
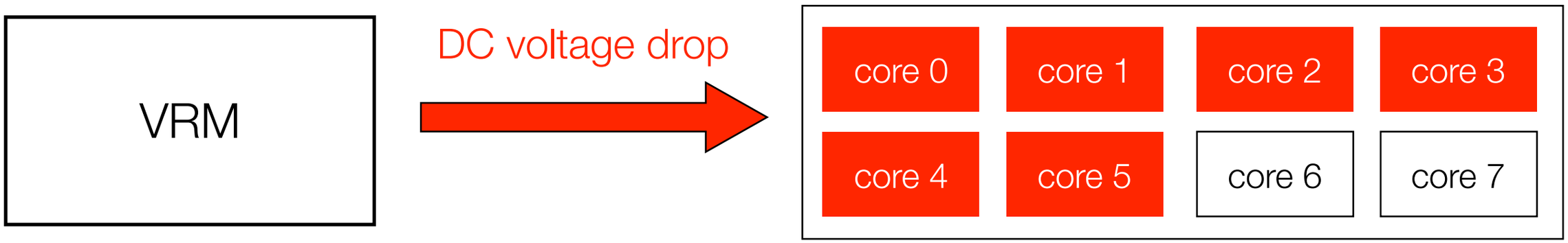


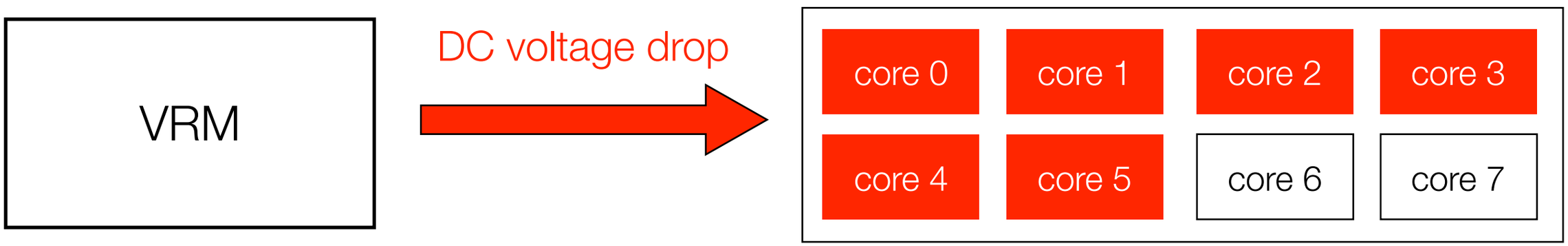
“Bank Run” on Active Timing Margin

- High-power workload induces DC voltage drop



“Bank Run” on Active Timing Margin

- High-power workload induces DC voltage drop
- Limit ATM’s timing margin reclamation potential



Adaptive Guardband Scheduling to Improve System-Level Efficiency of the POWER7+

Yazhou Zu[1], Charles R. Lefurgy[2], Jingwen Leng[1], Matthew Halpern[1],
Michael S. Floyd[2], Vijay Janapa Reddi[1]

[1] The University of Texas at Austin
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ABSTRACT

The traditional guardbanding approach to ensure processor reliability is becoming obsolete because it always over-provisions voltage and wastes a lot of energy. As a next-generation alternative, adaptive guardbanding dynamically adjusts chip clock frequency and voltage based on timing margin measured at runtime. With adaptive guardbanding, voltage guardband is only provided when needed, thereby promising significant energy efficiency improvement.

In this paper, we provide the first full-system analysis of adaptive guardbanding's implications using

Categories and Subject Descriptors

B.8 [**Hardware**]: Performance and Reliability; C.1.0 [**Processor Architectures**]: General

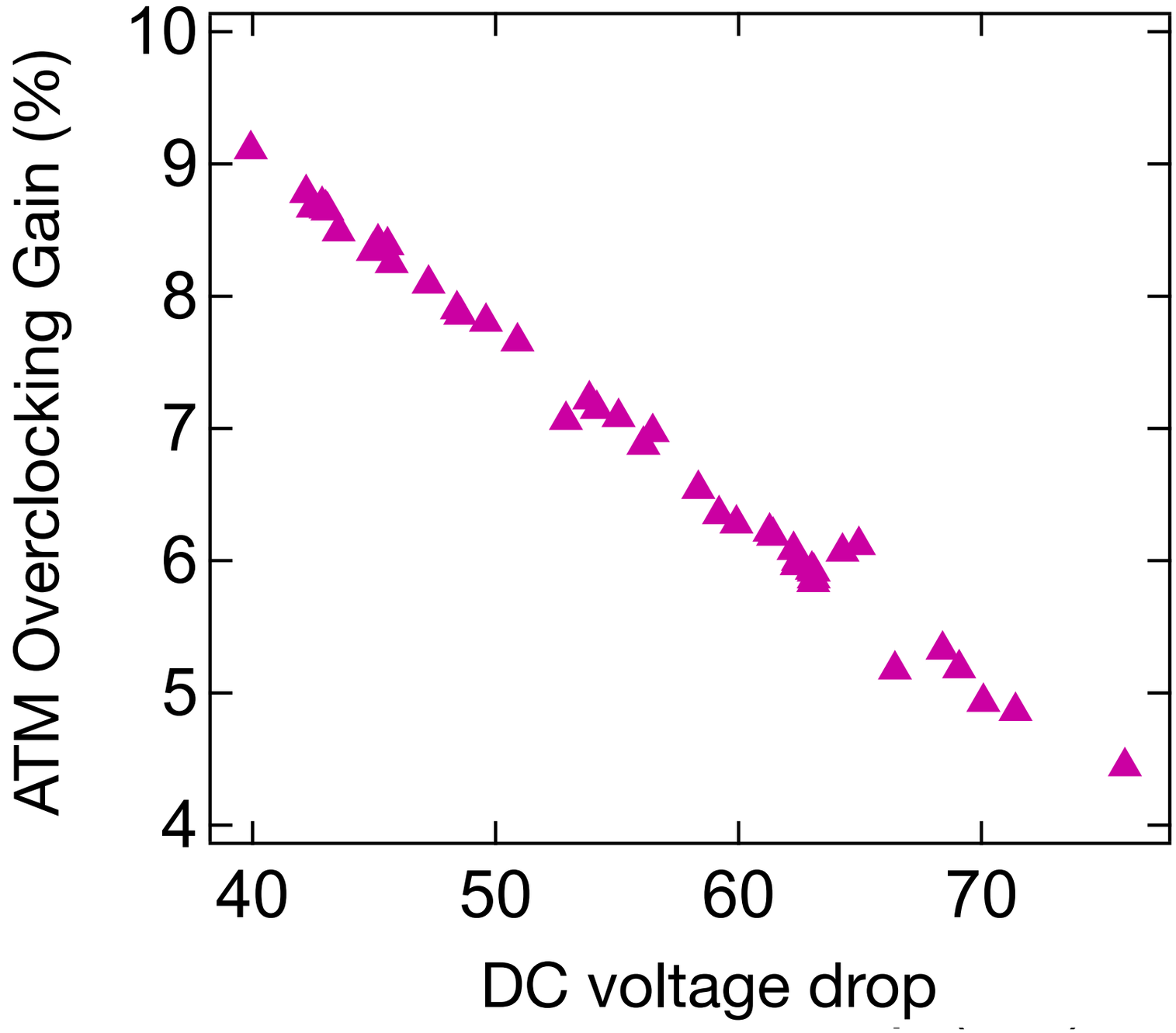
Keywords

operating margin; di/dt effect; voltage drop; energy efficiency; scheduling

1. INTRODUCTION

Processor manufacturers commonly apply operating guardband to ensure that microprocessors operate reli-

Application Power Consumption Limits ATM's Gain



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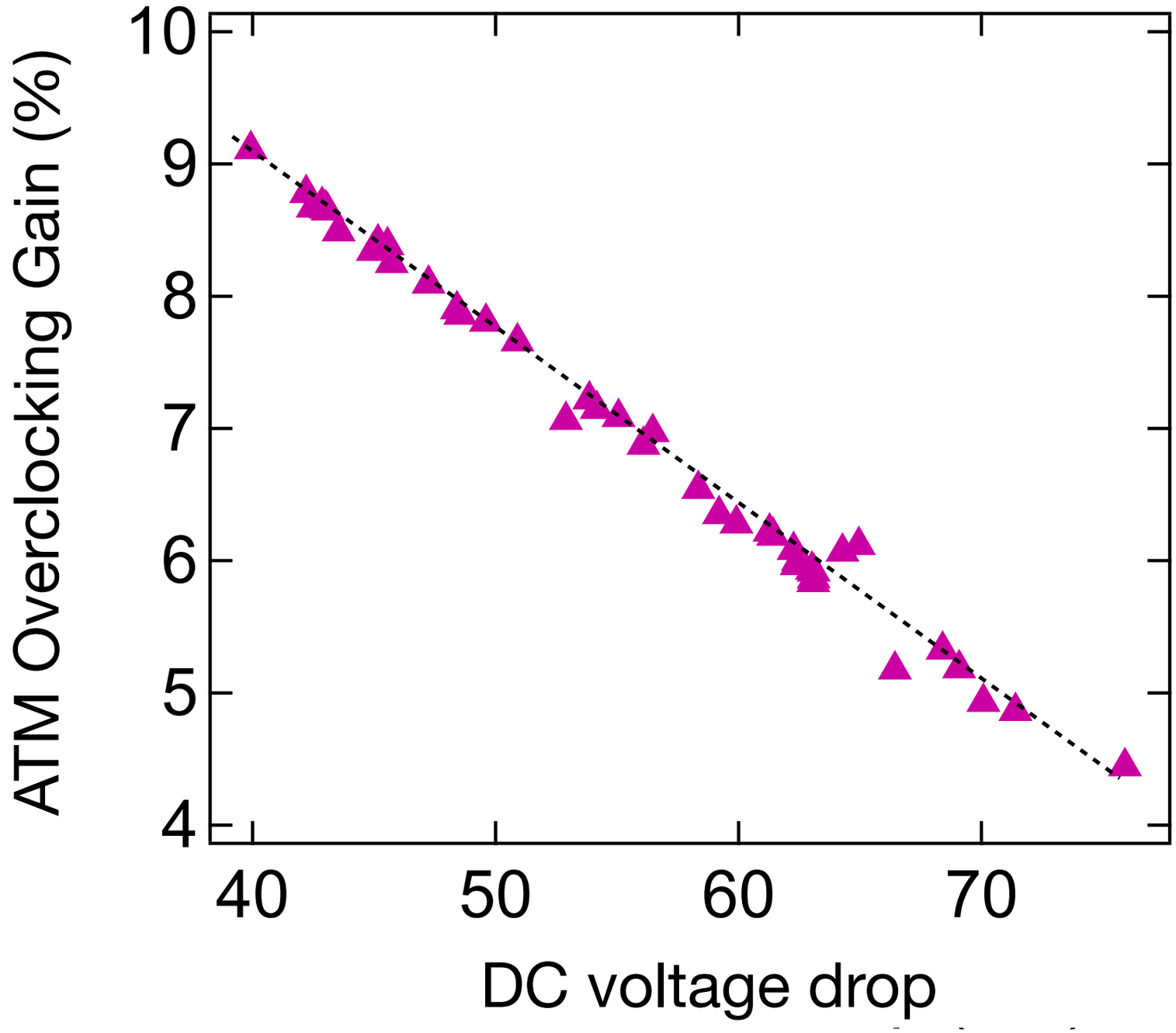

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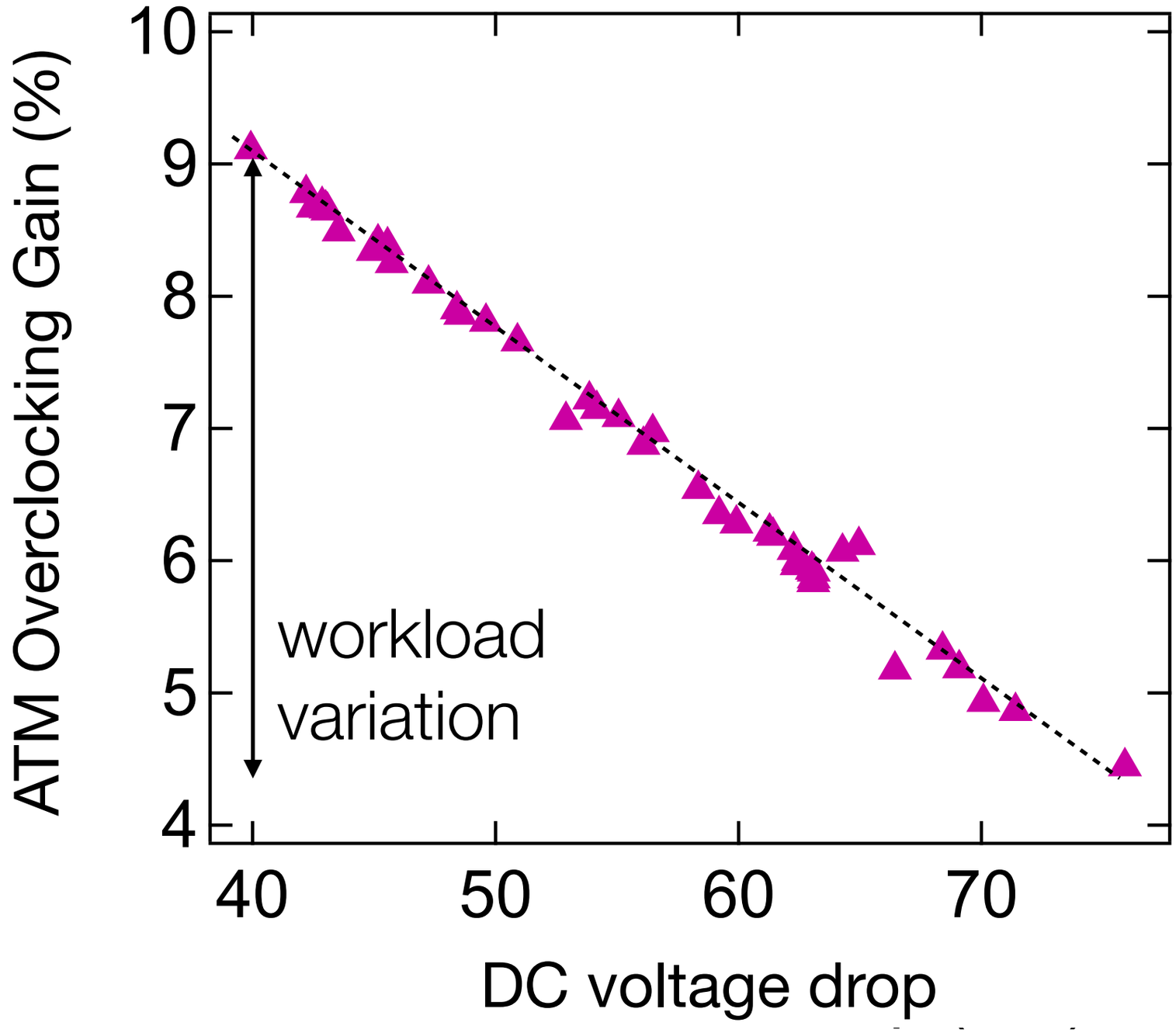
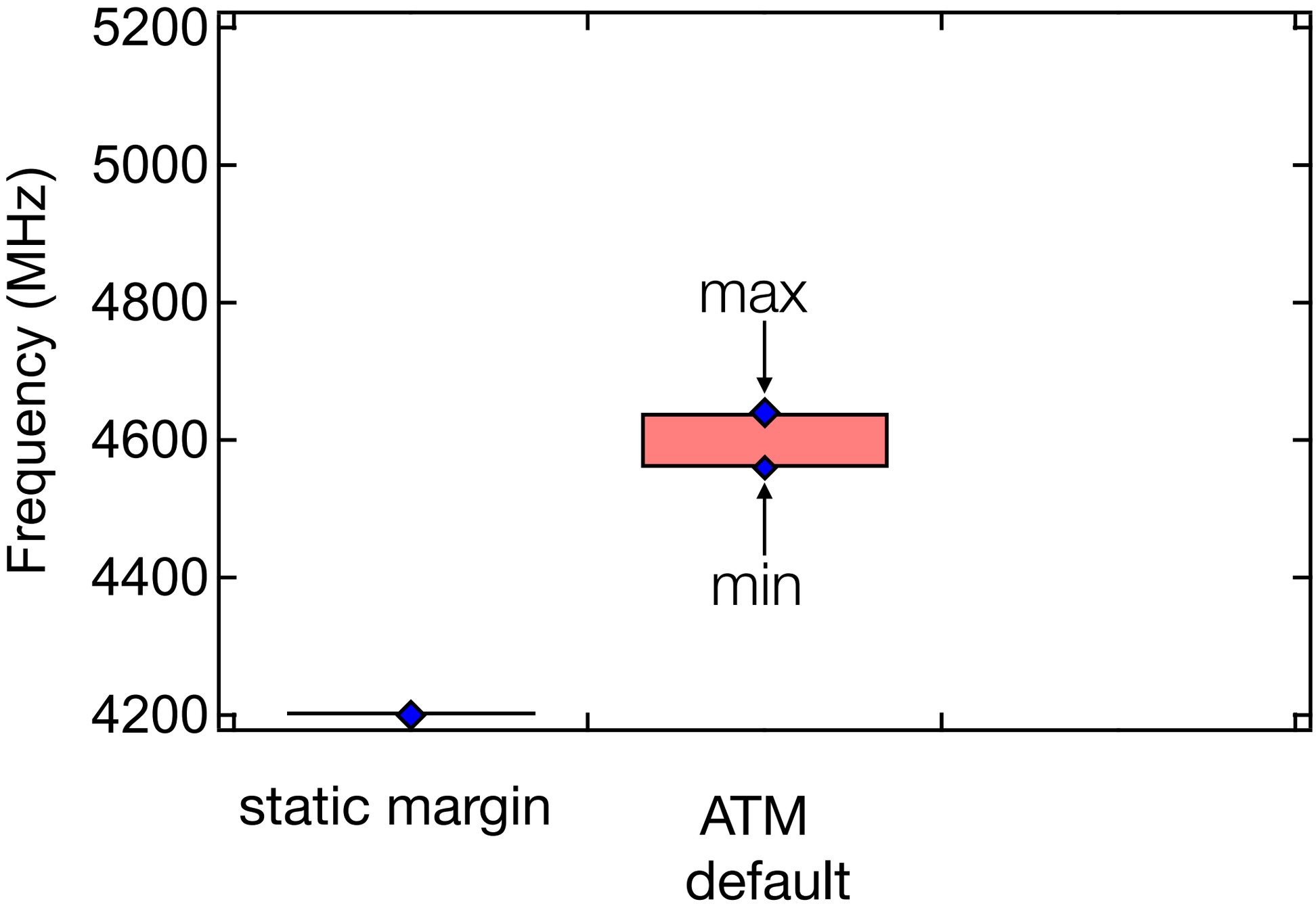


Executive Summary



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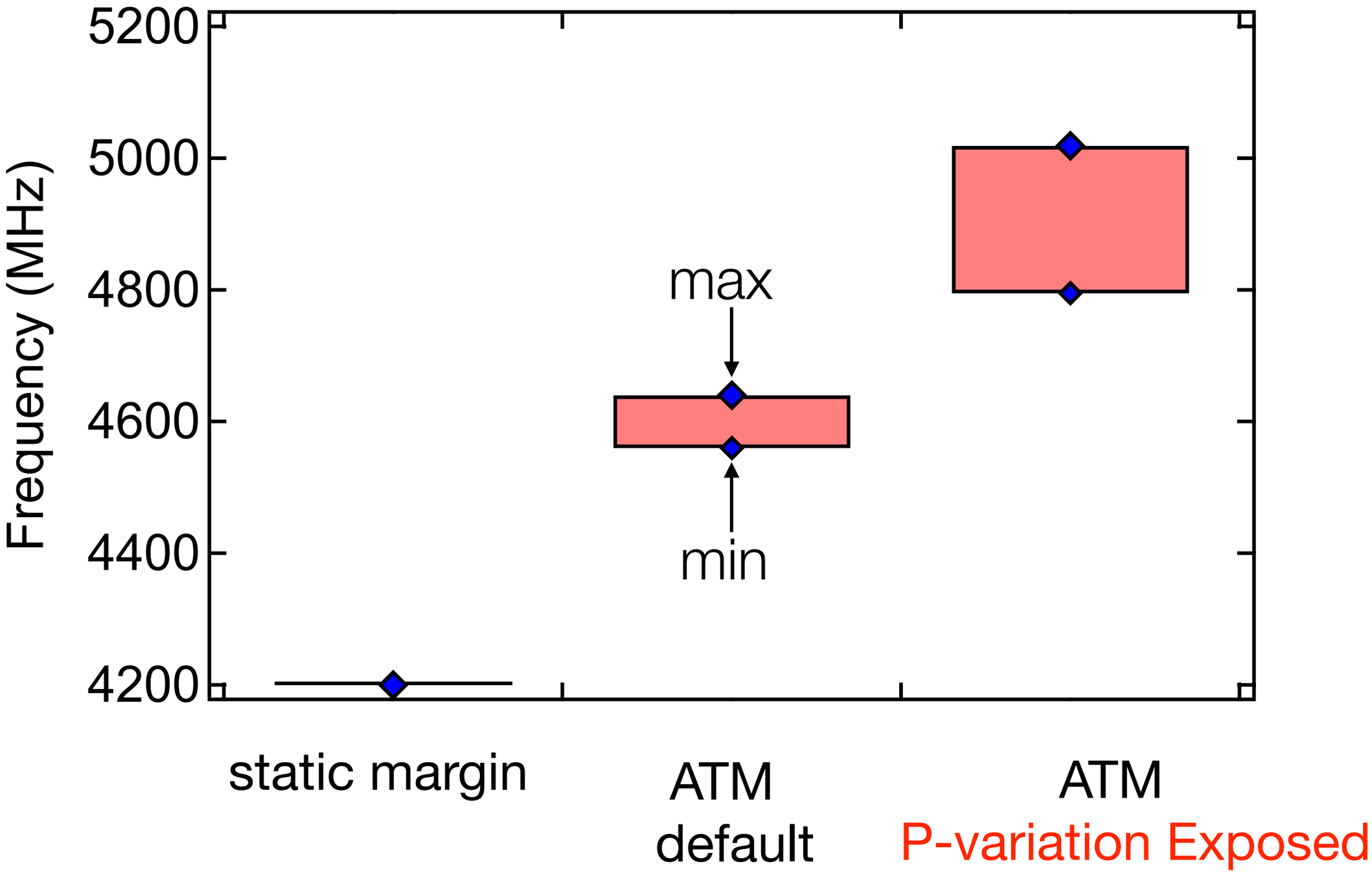

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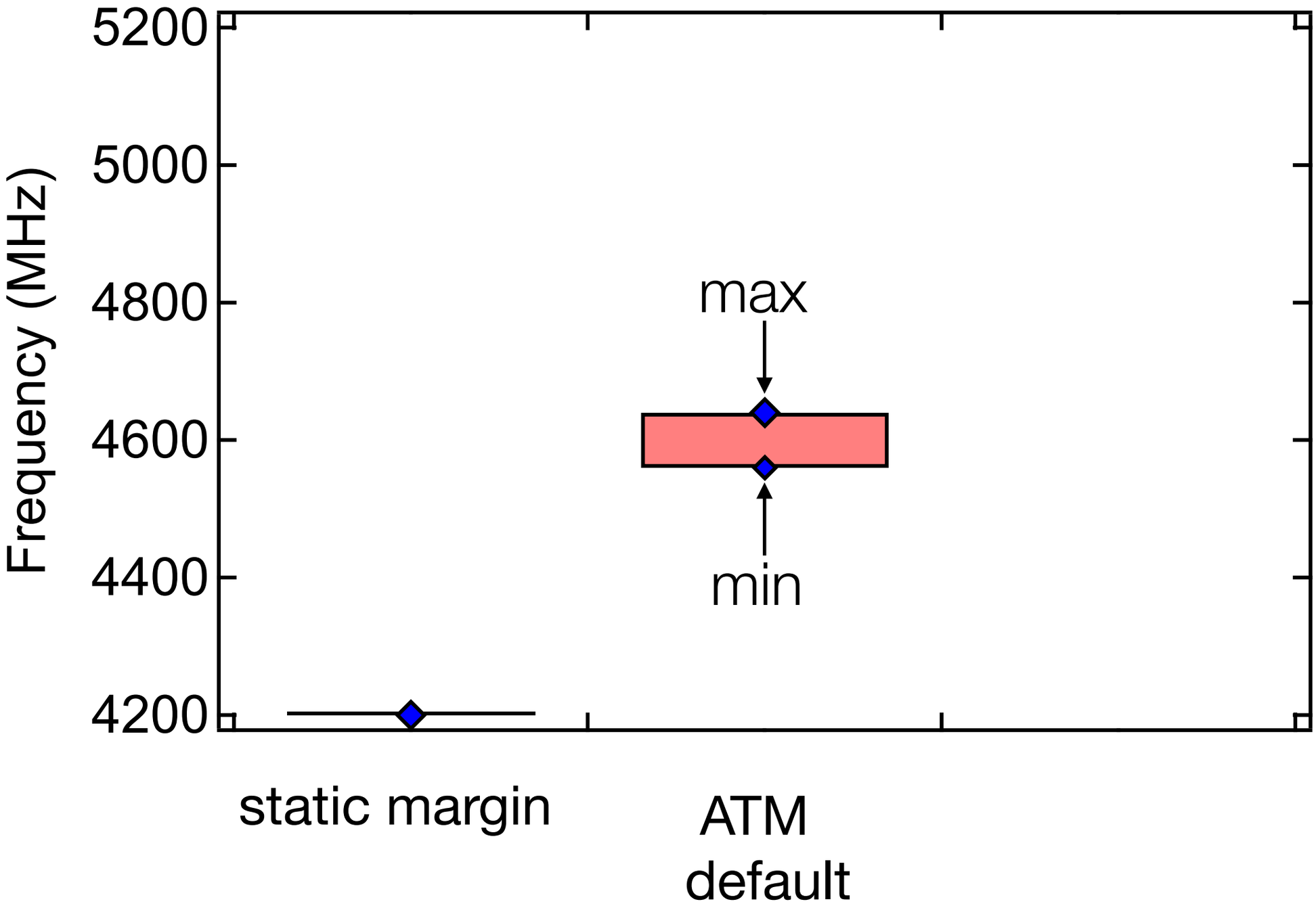

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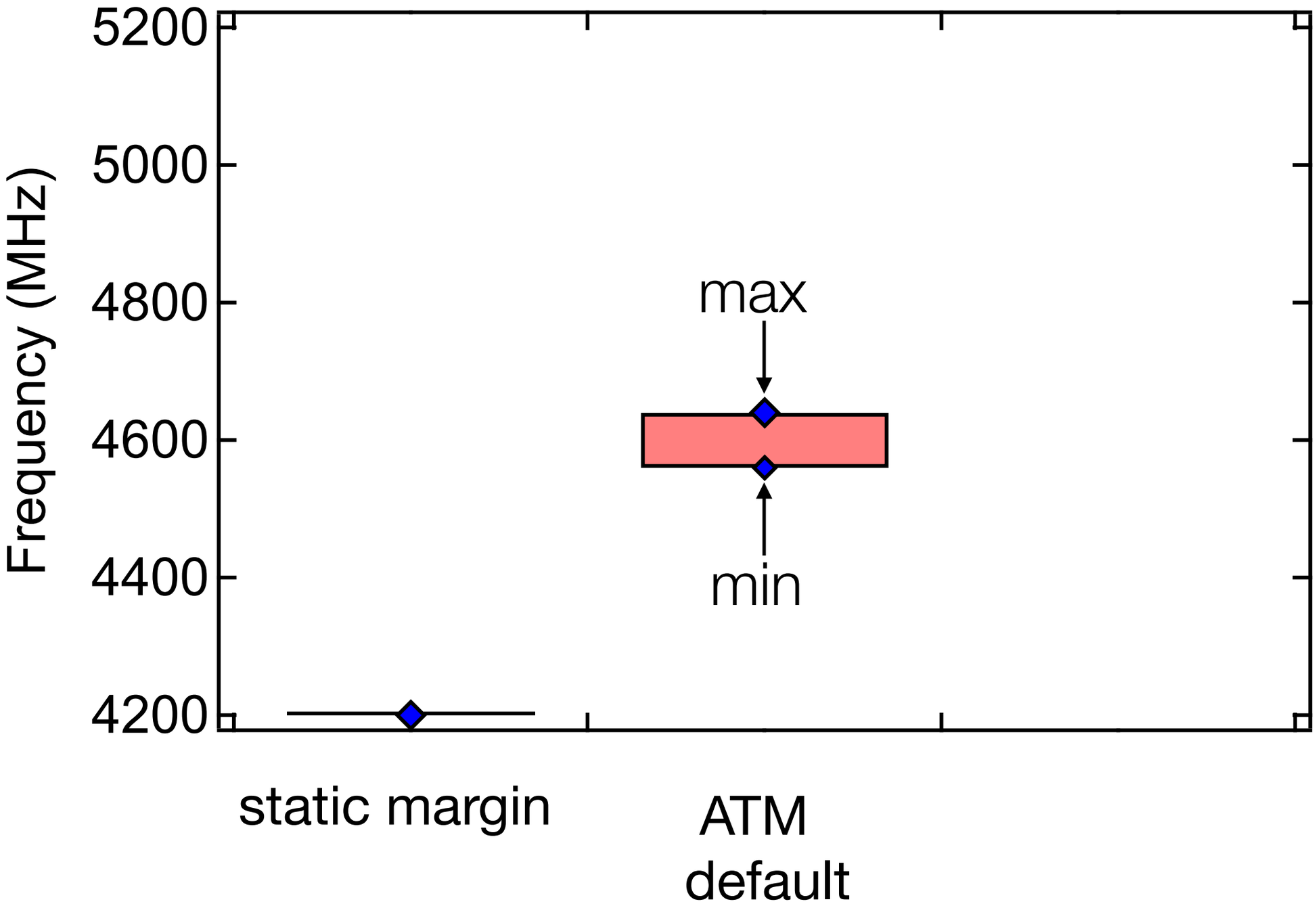

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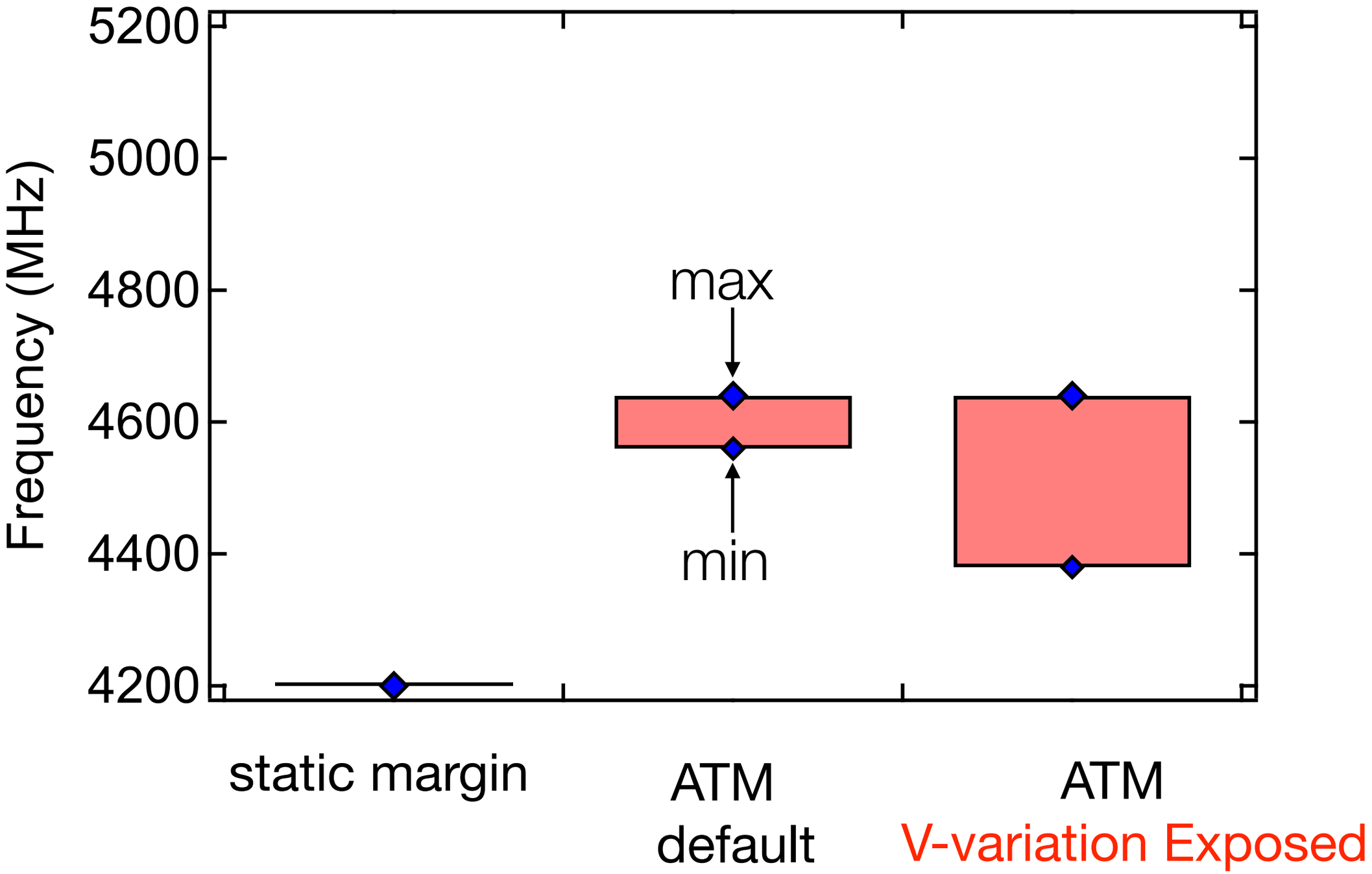

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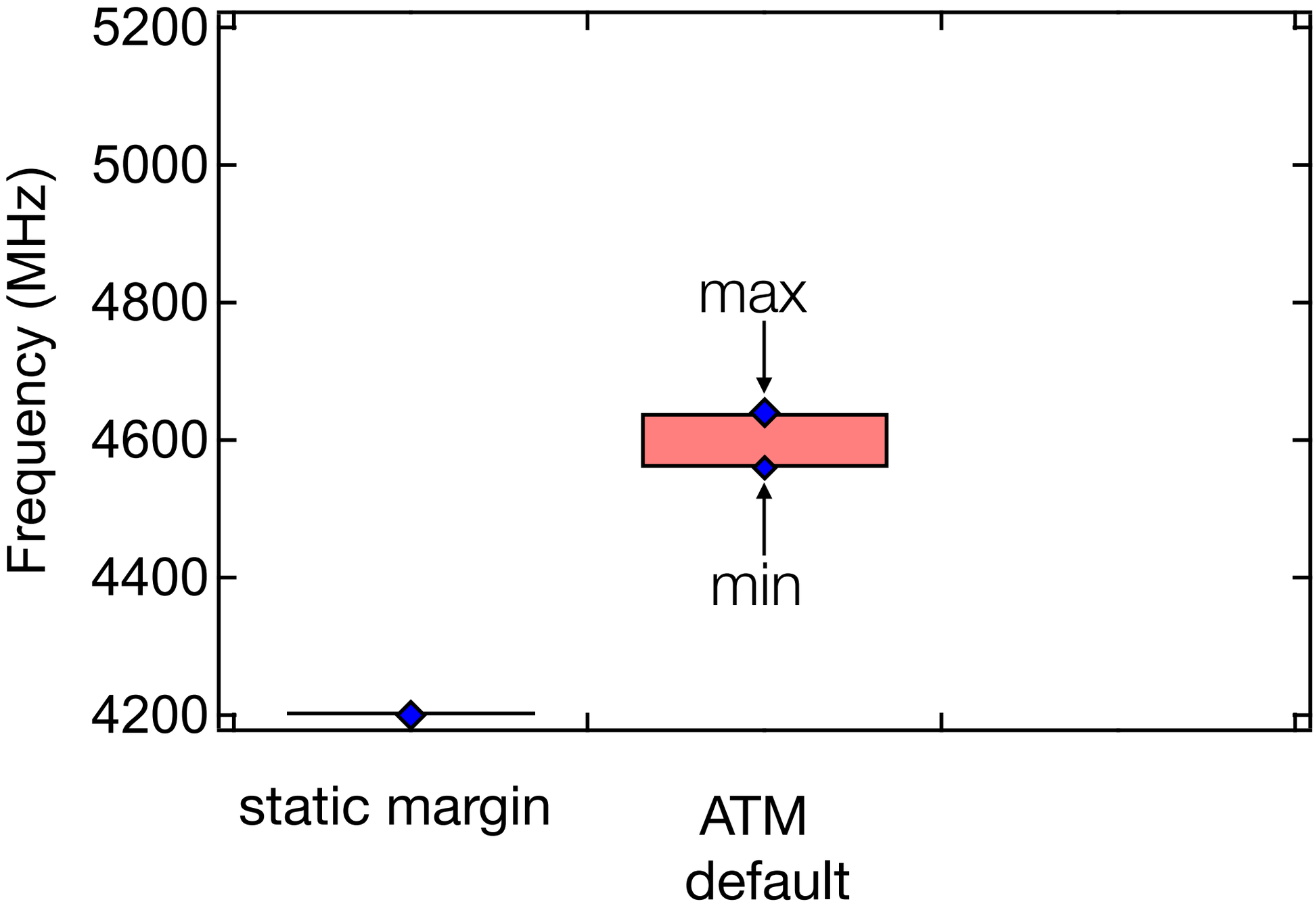

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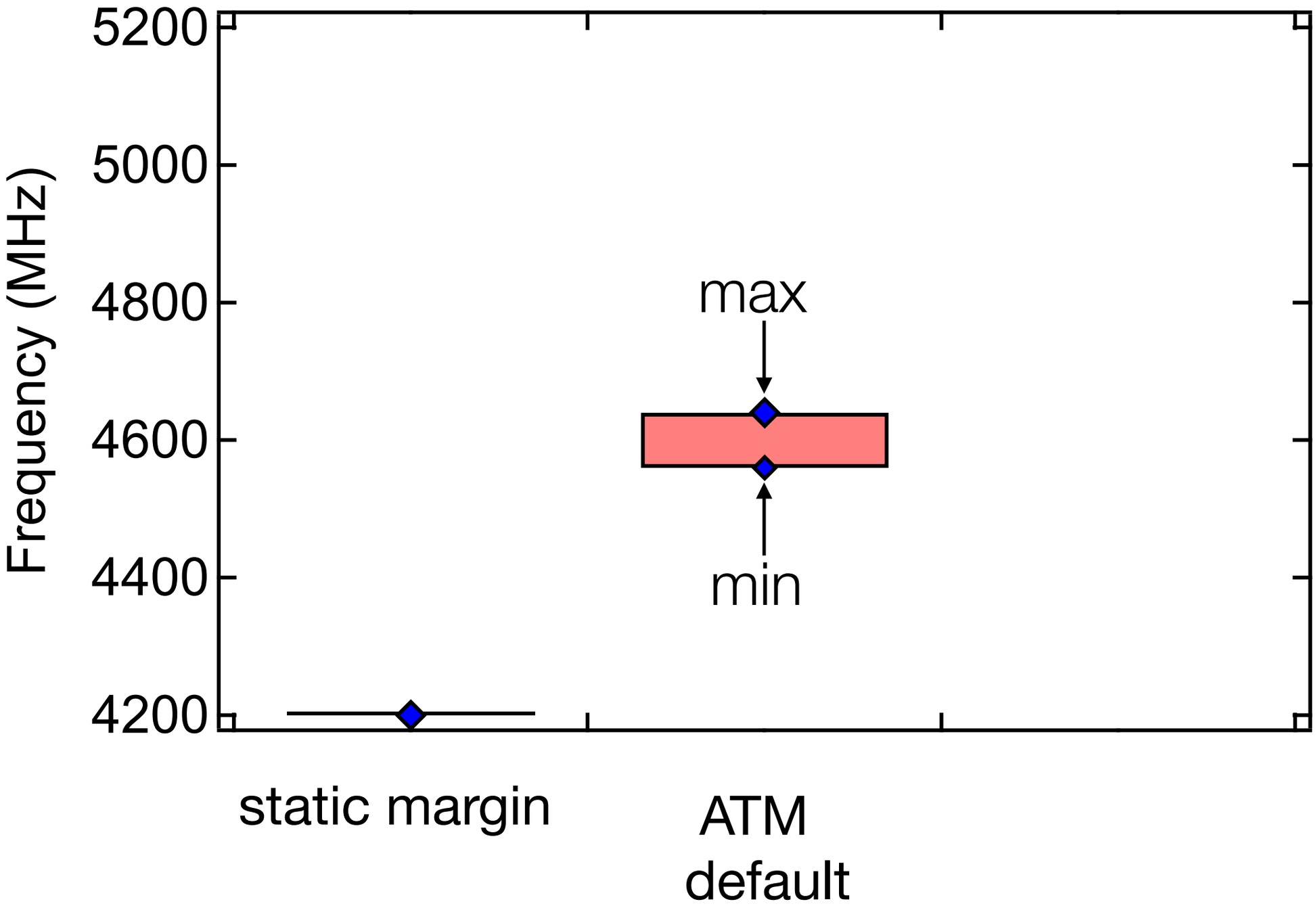

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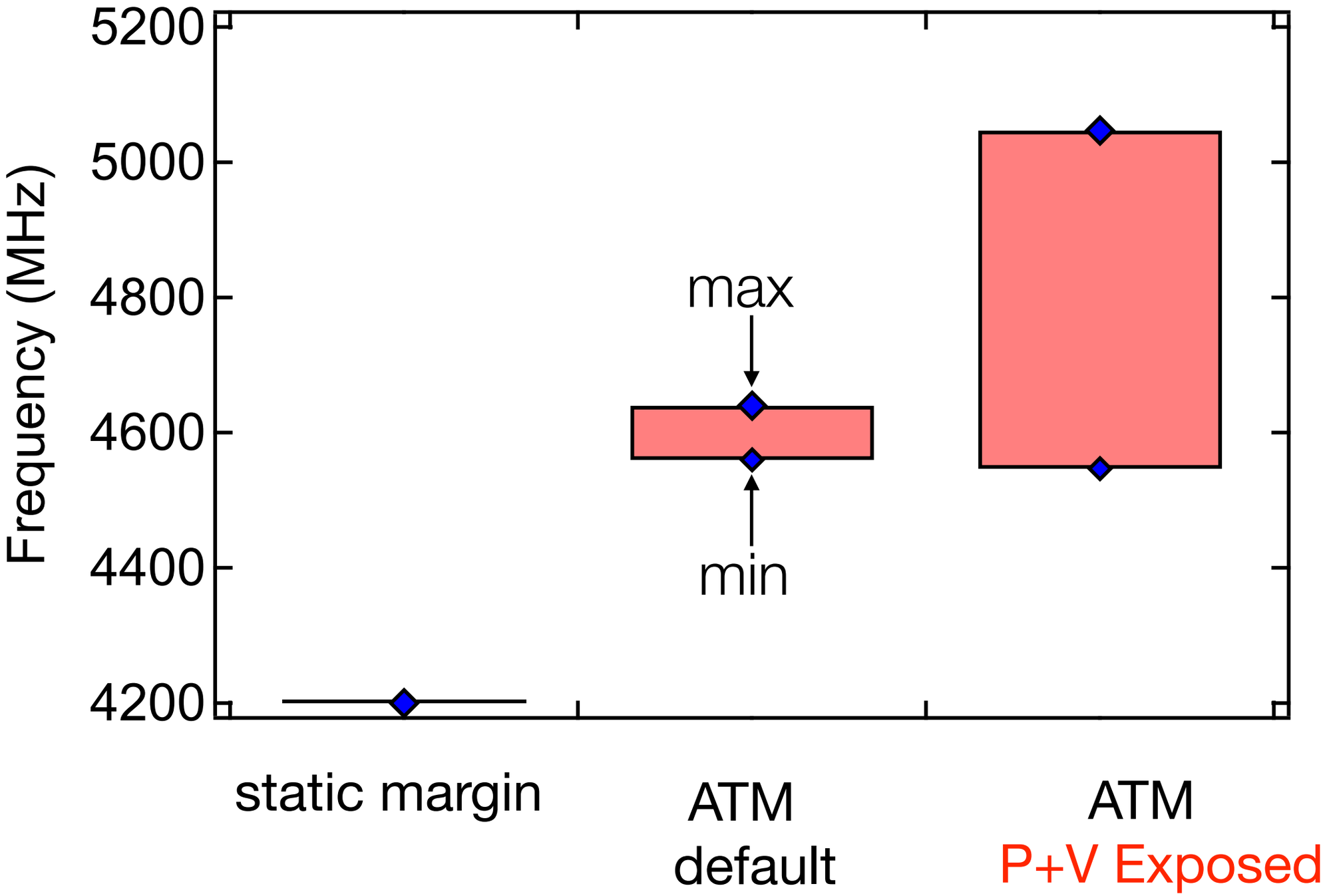

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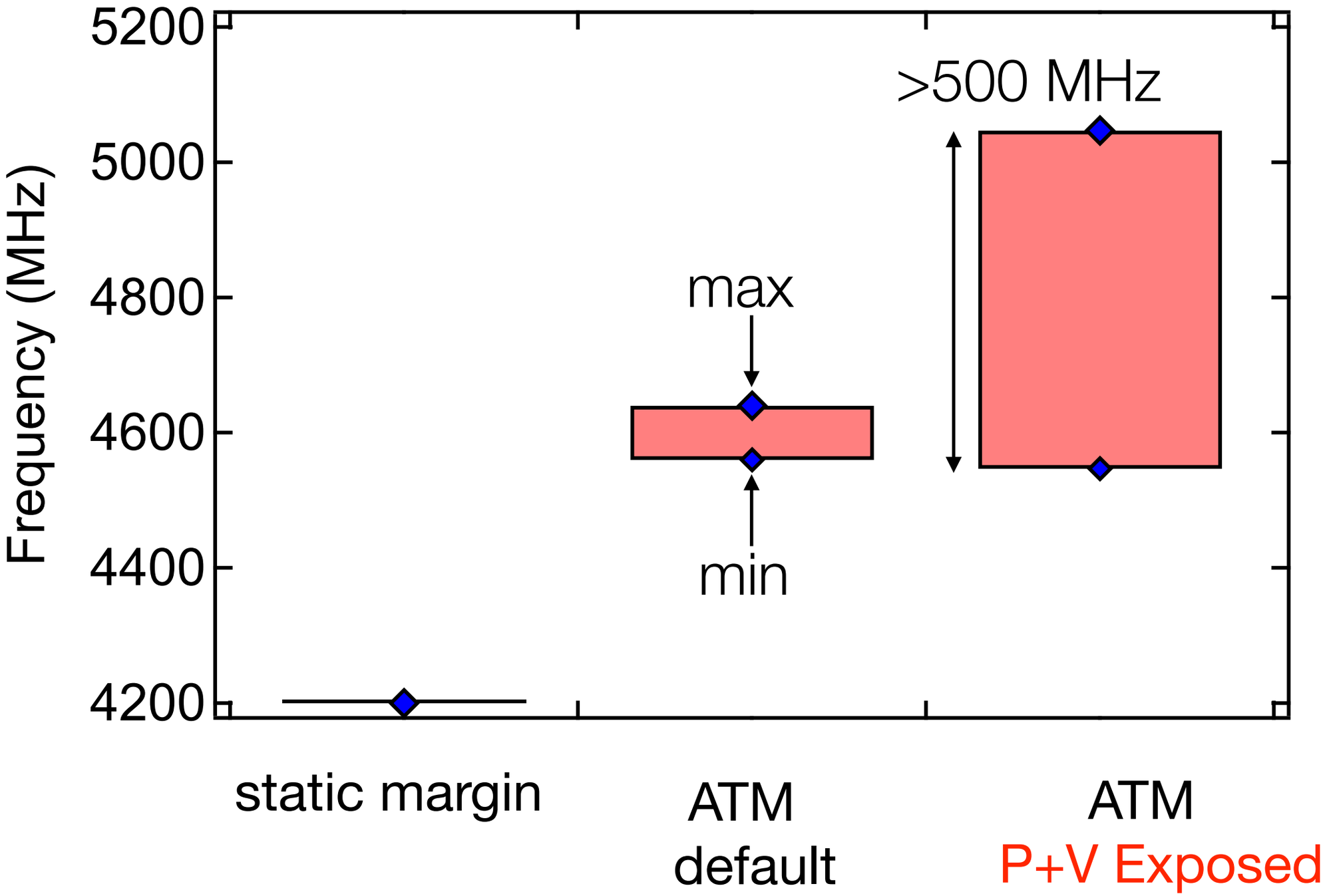

Executive Summary

- Fine-tune core-level ATM to **automatically** expose inter-core performance variation

- Expose chip-wide performance variation caused by heterogenous workload intensity

- Propose application management to demonstrate >10% predictable performance gain

Managing Cloud Workload Performance

- Latency, not frequency, matters for cloud workloads

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Foreground (fg)	Background (bg)
resnet, vgg, ferret, fluidanimate	mlp-train, gcc, facesim, lu_cb, streamcluster
squeezenet, seq2seq, babi-rnn, bodytrack, vips	blackscholes, x264 swaptions, raytrace

Managing Cloud Workload Performance

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latency-sensitive, user-facing services

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- Latency, not frequency, matters for cloud workloads
- Improve foreground critical workload performance controllably

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latency-sensitive, user-facing services

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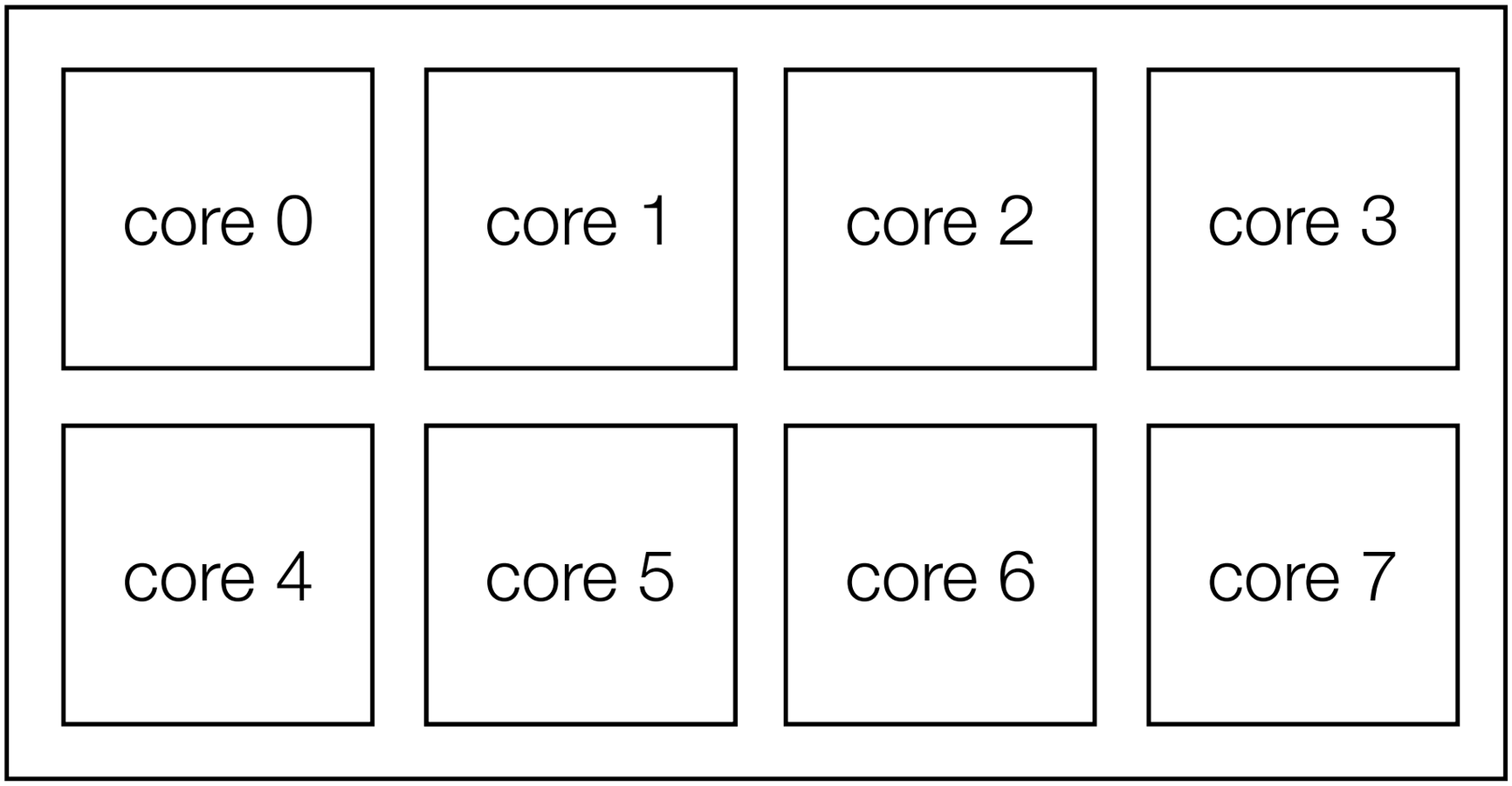
memory intensive	resnet, vgg, ferret, fluidanimate	mlp-train, gcc, facesim, lu_cb, streamcluster
memory non-intensive	squeezenet, seq2seq, babi-rnn, bodytrack, vips	blackscholes, x264 swaptions, raytrace

Managing Critical Application Performance



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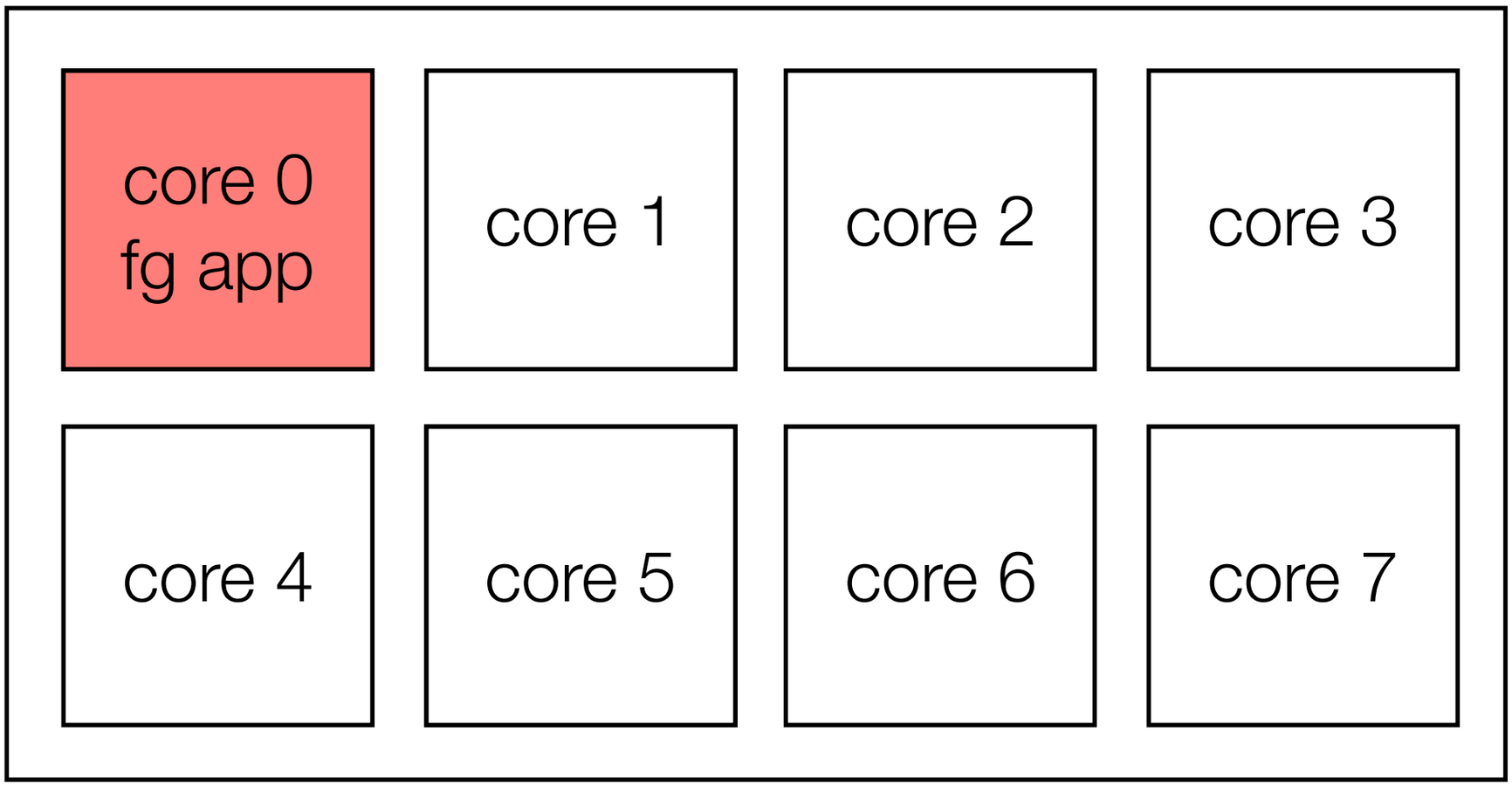

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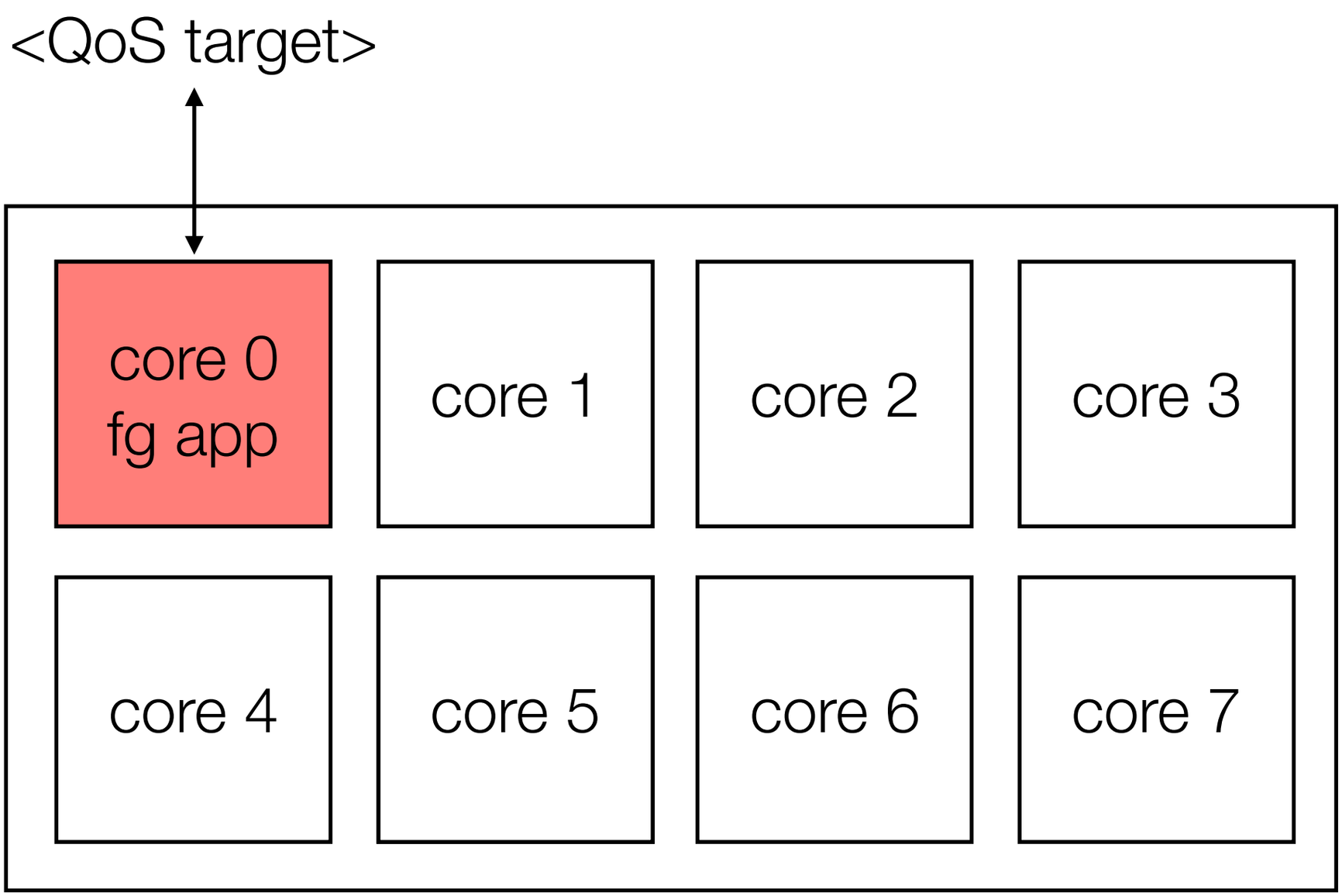

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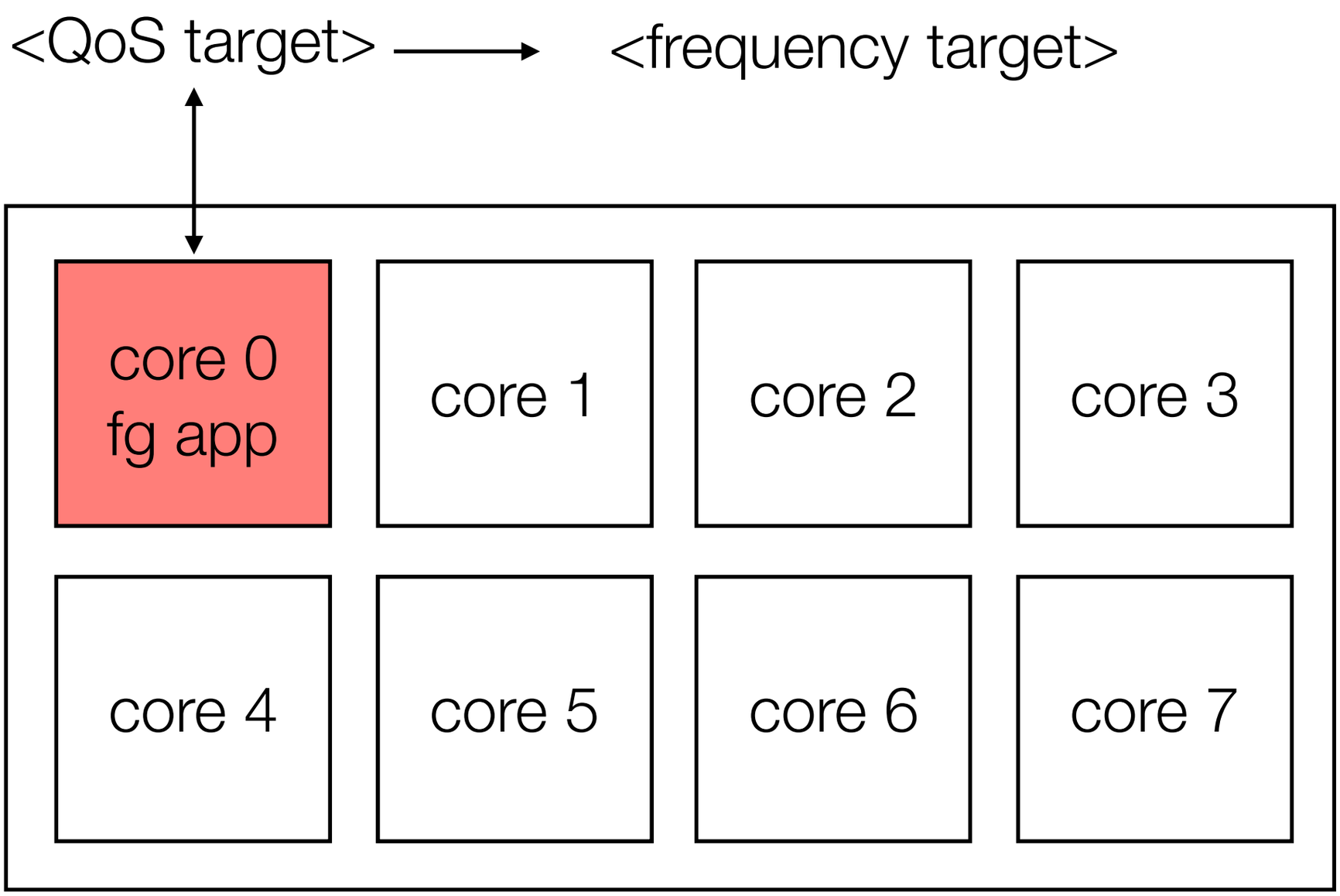

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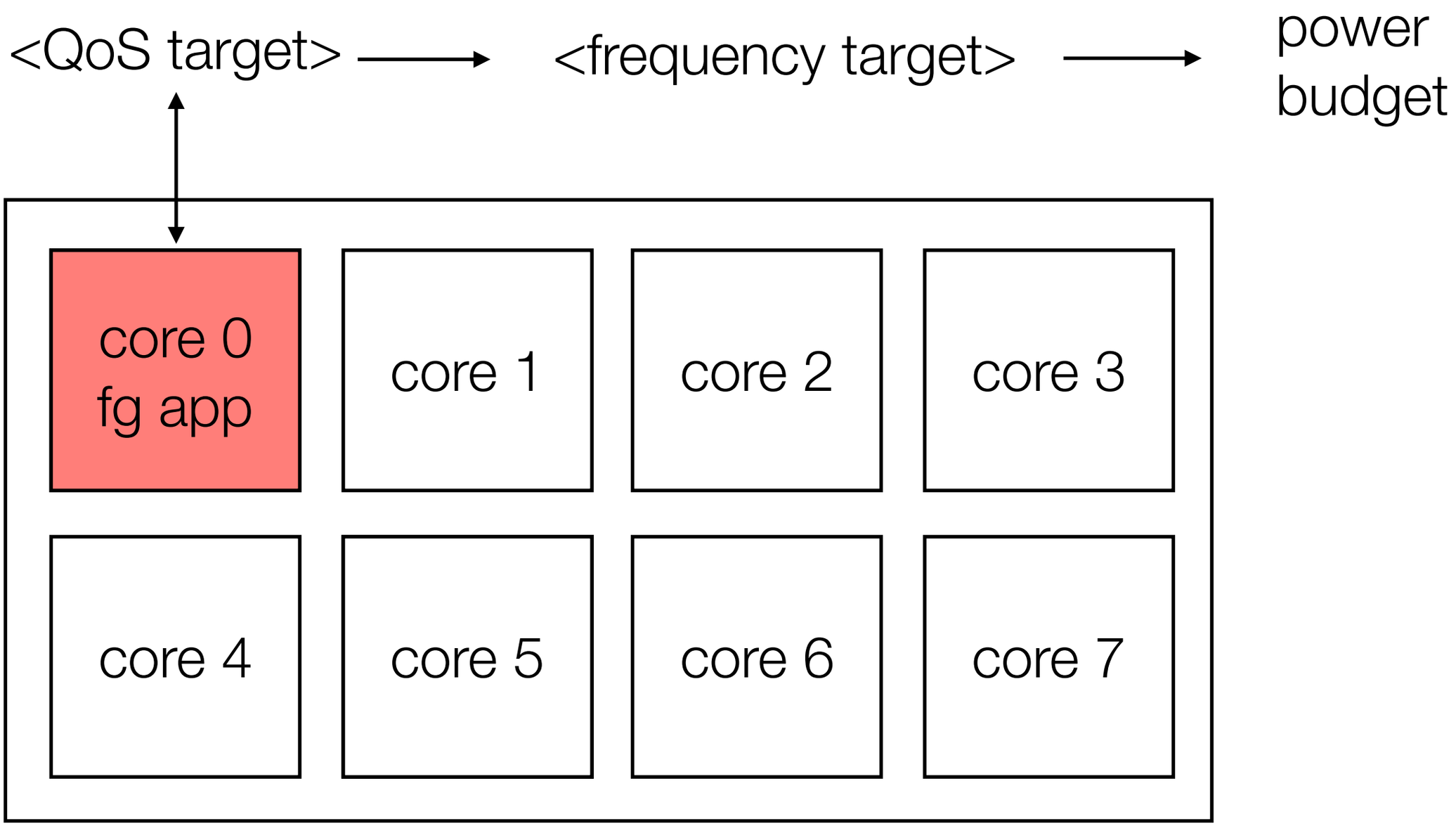

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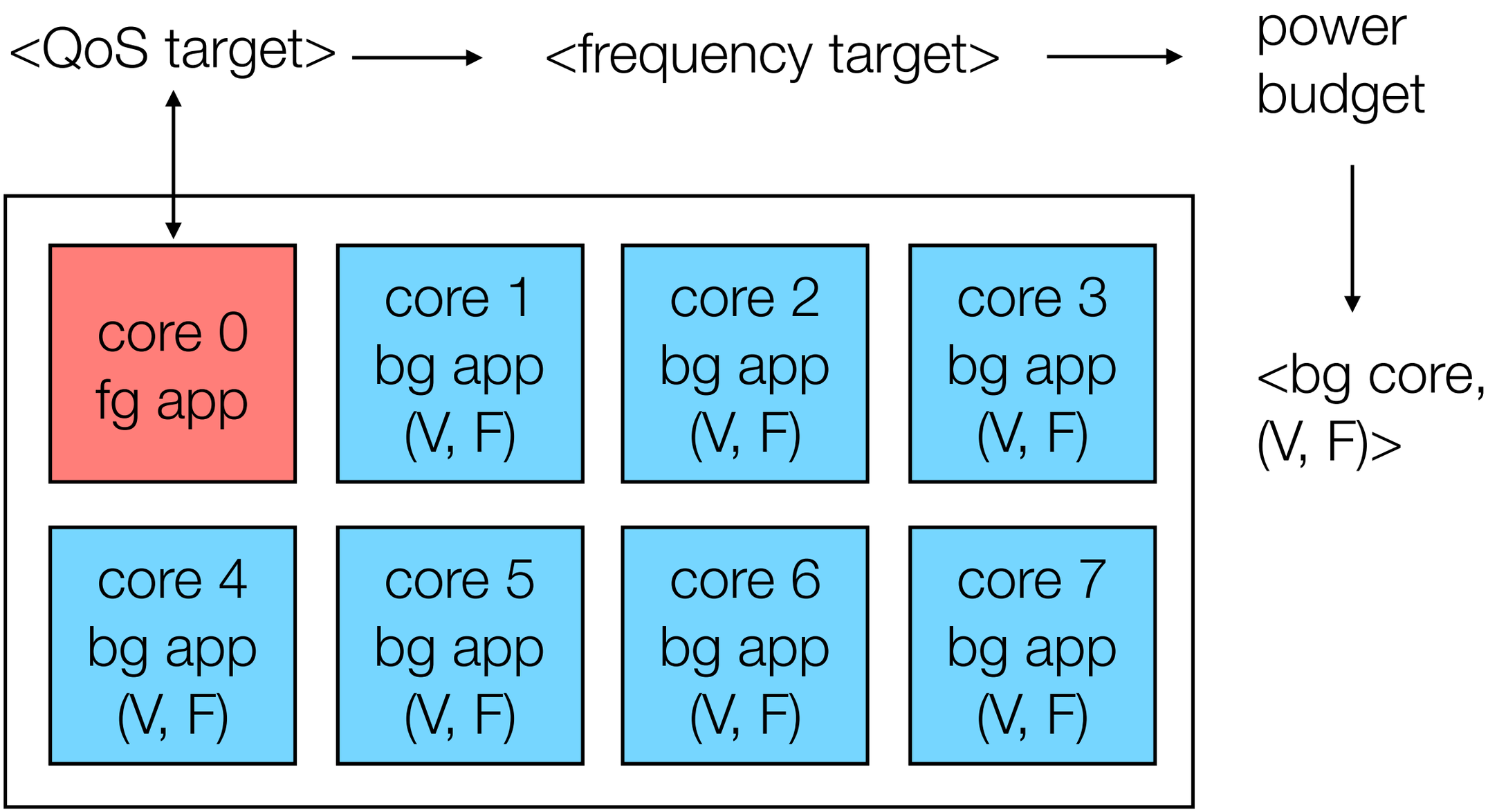
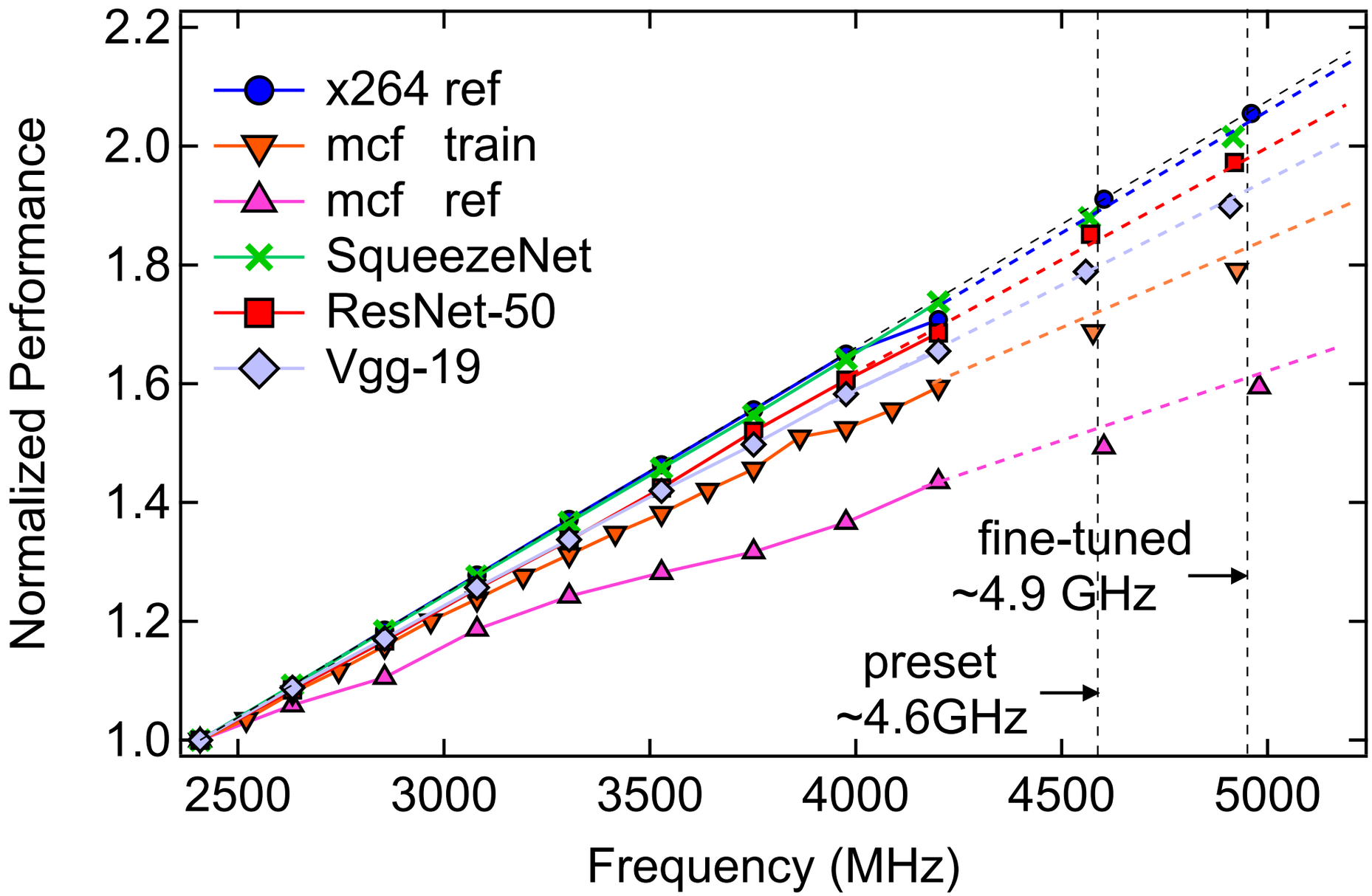


Frequency-based Performance Predictor

- Linear predictor profiled by application and input size



Power-based ATM Frequency Predictor

$$\overline{f} = k \cdot \overline{V_{chip}}$$

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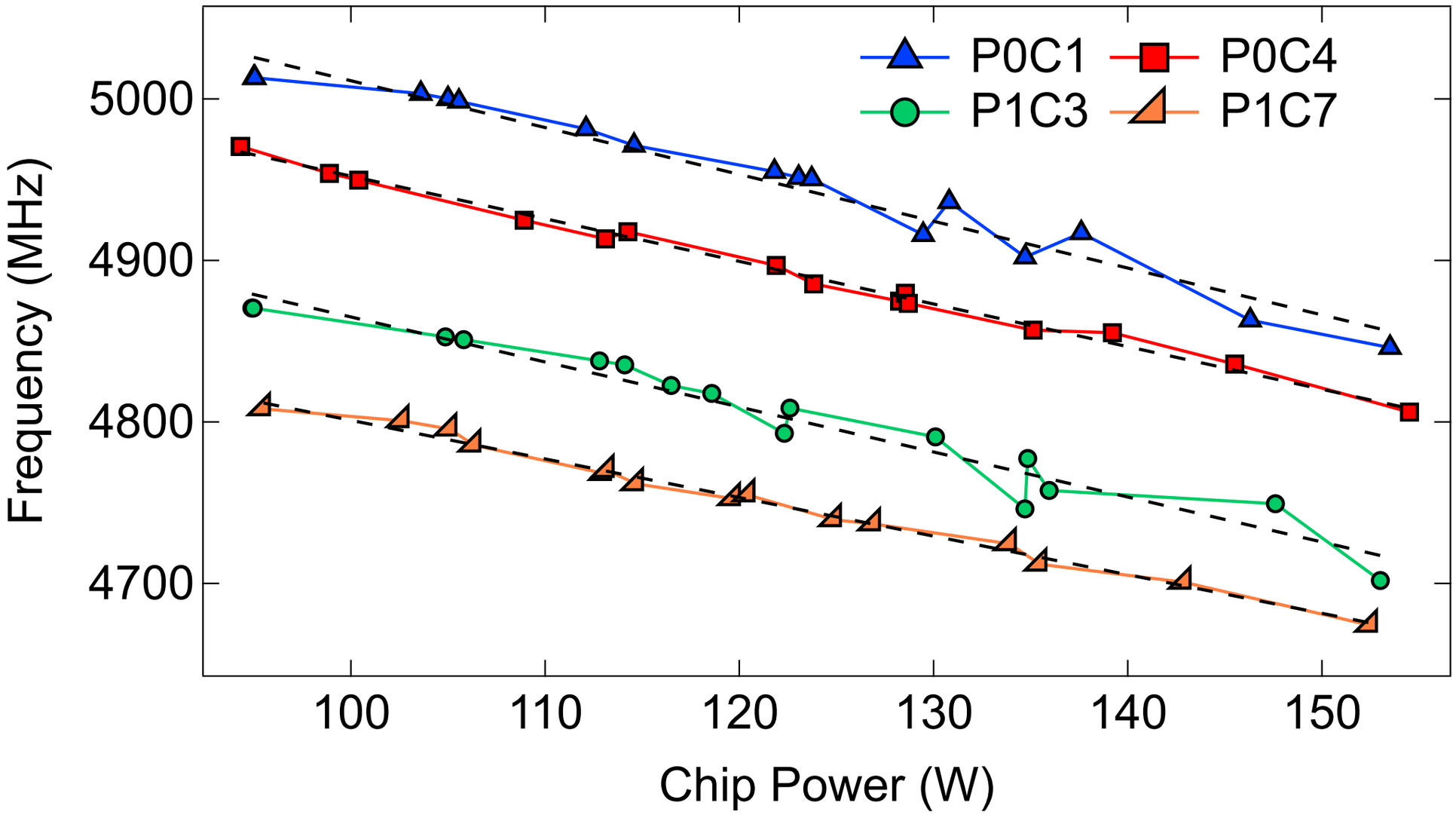

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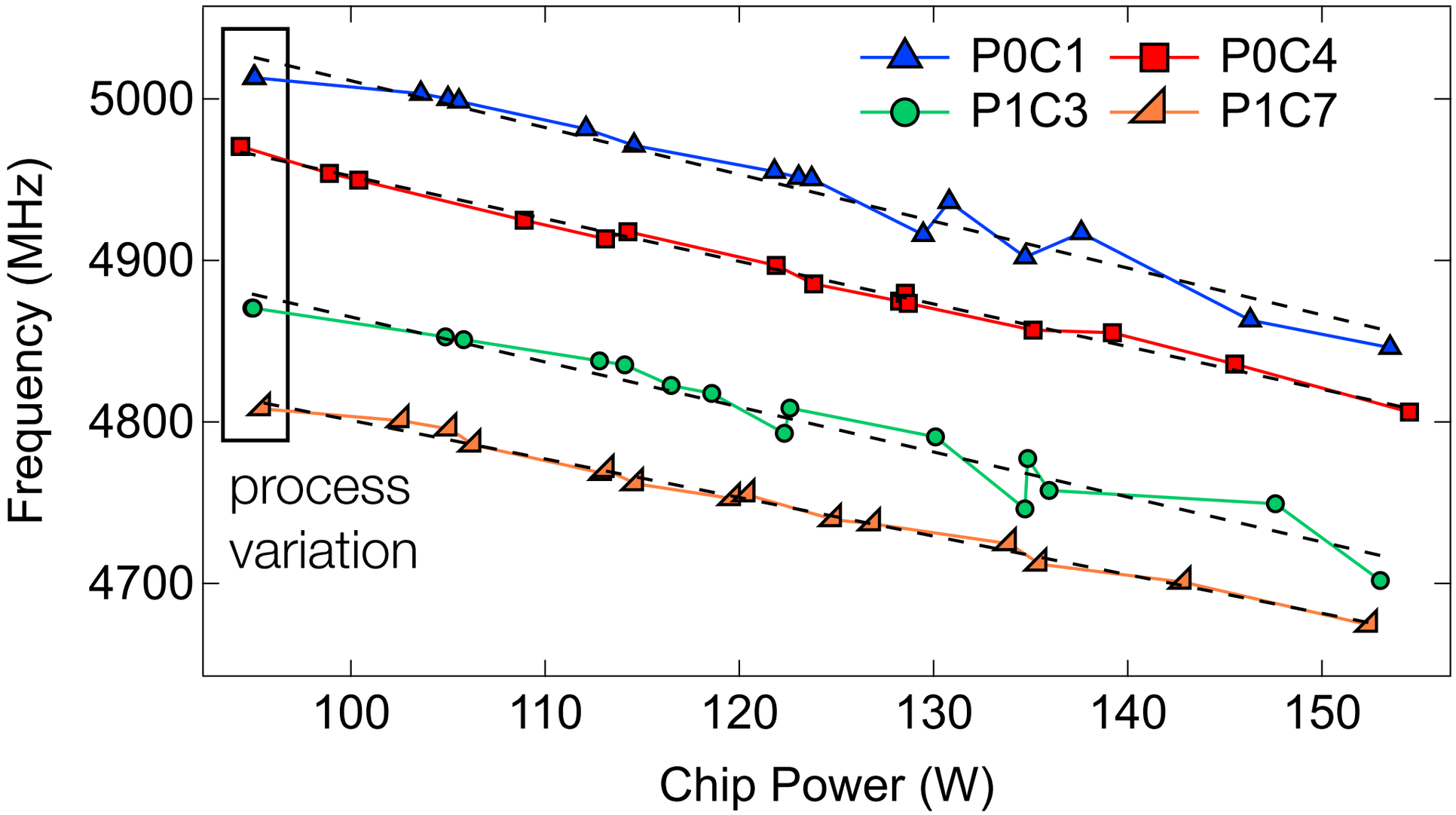

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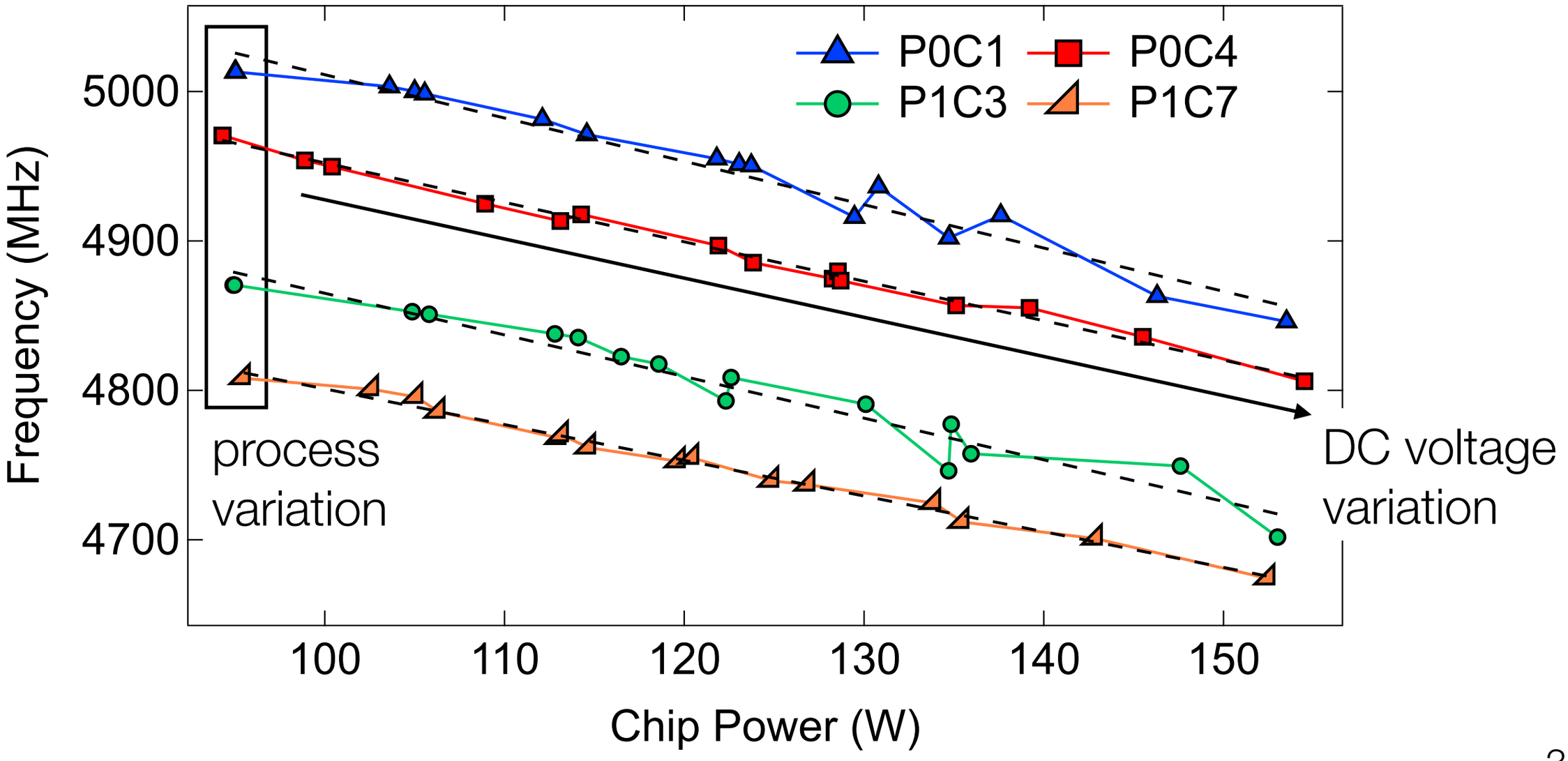
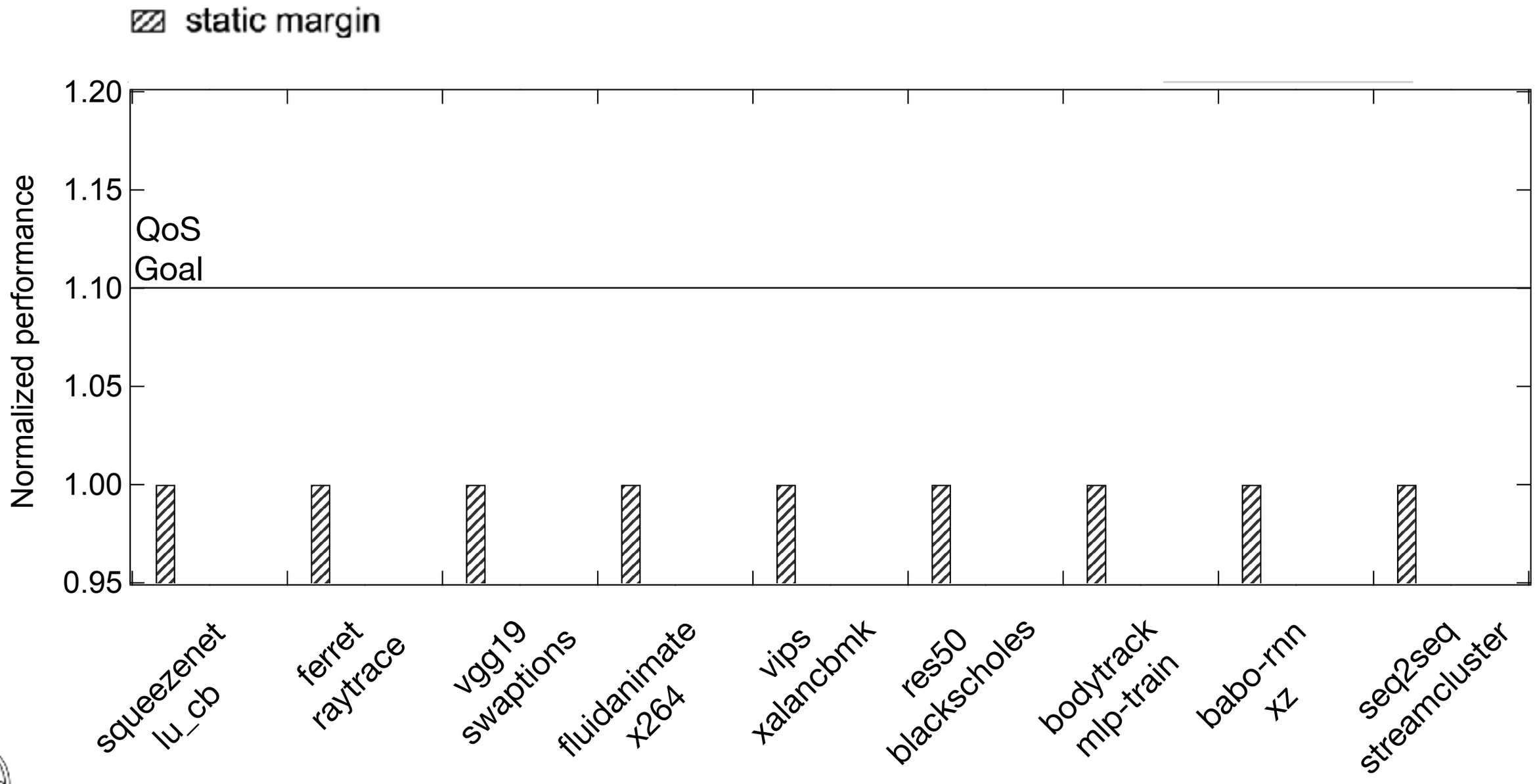


Performance Improvement



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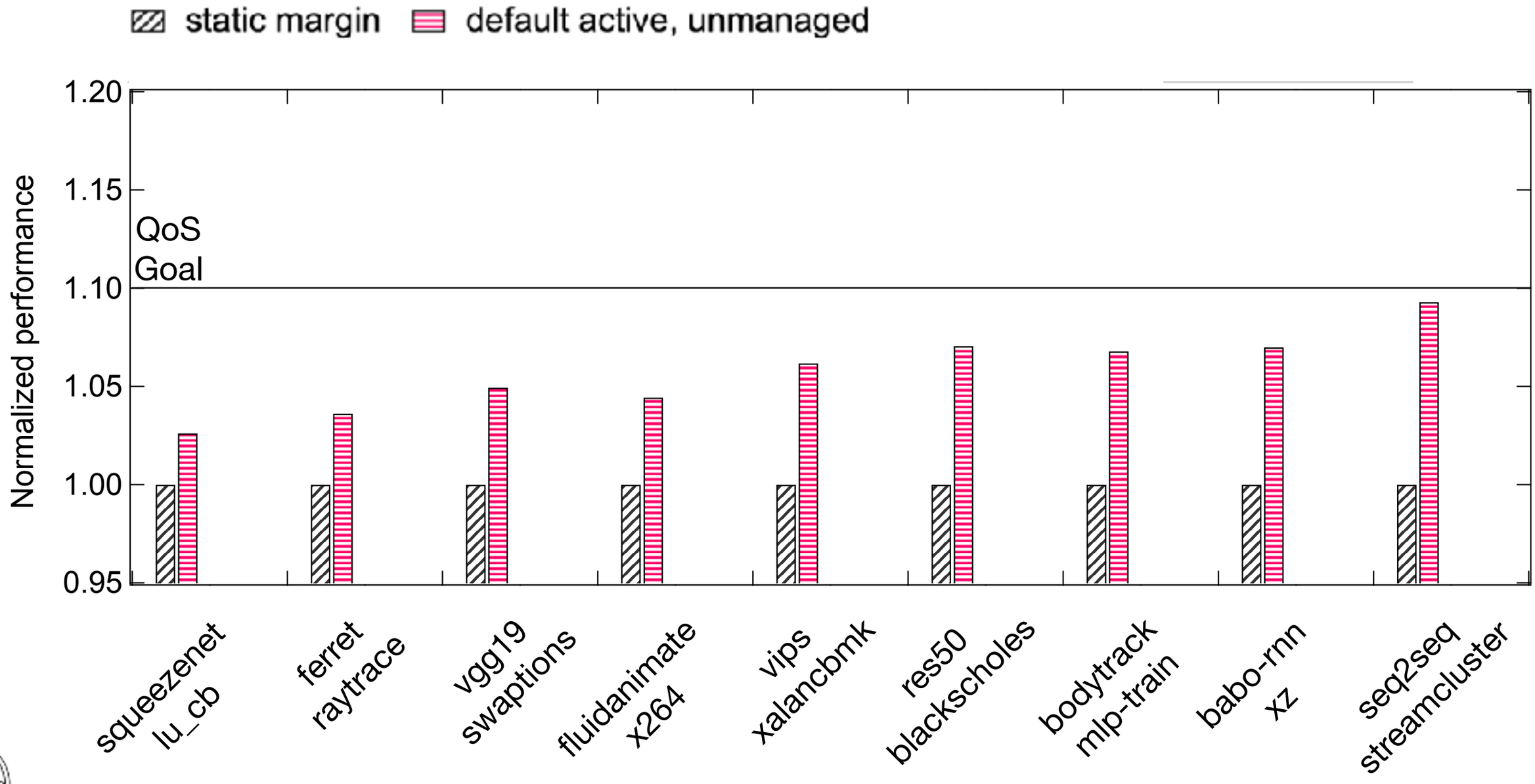
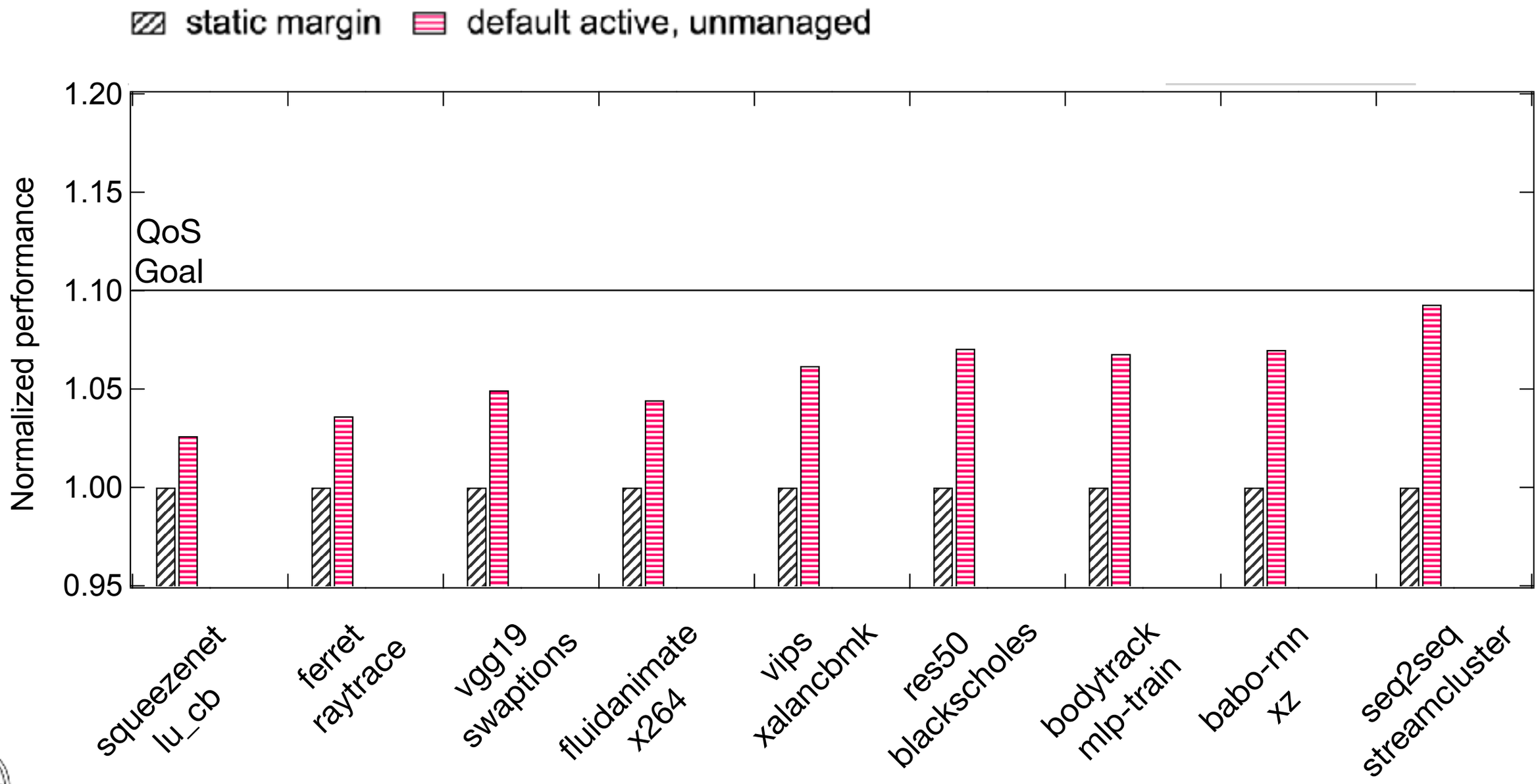


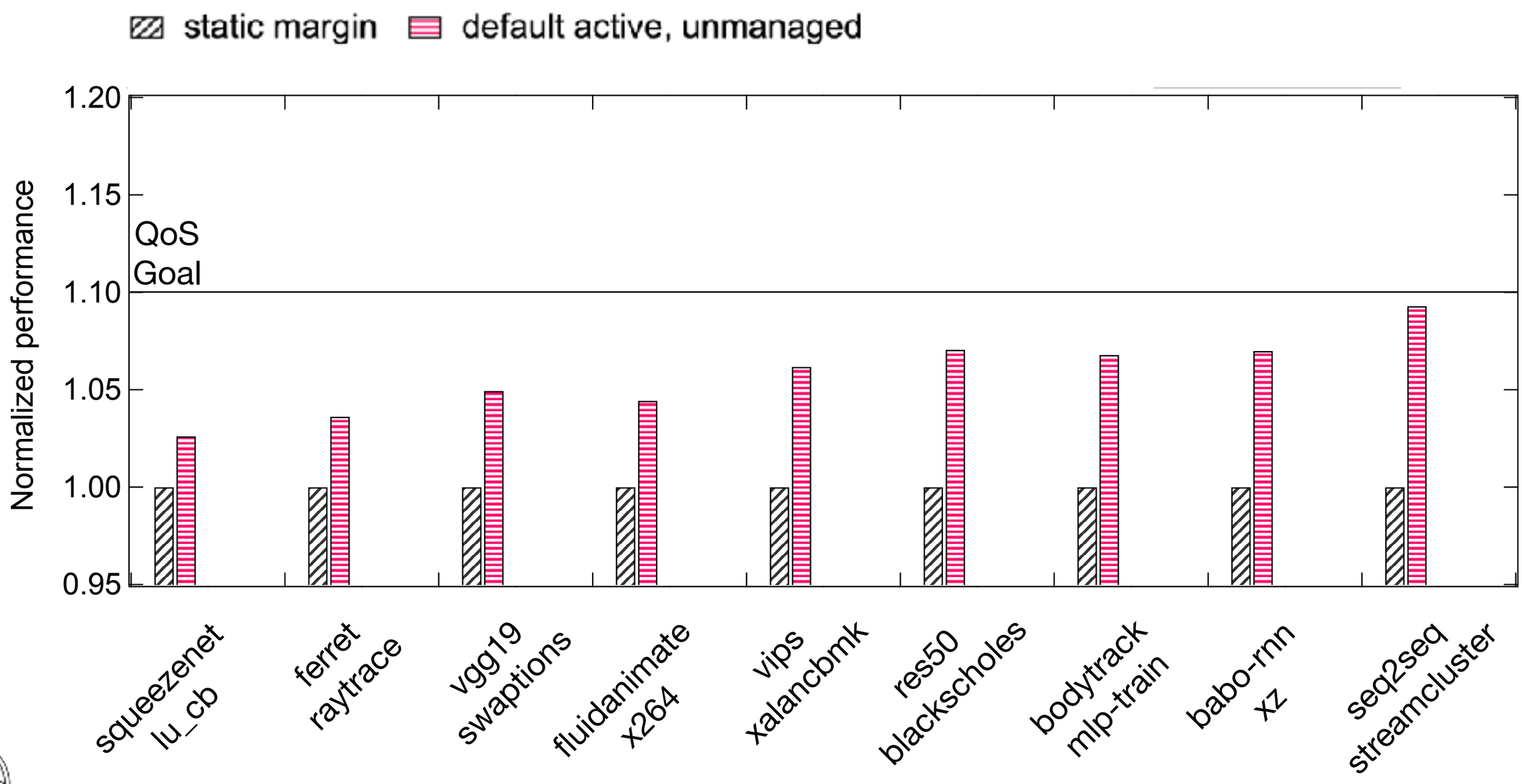
Performance Improvement

- Unmanaged DC voltage drop from co-runner apps



Performance Improvement

- Unmanaged DC voltage drop from co-runner apps
- 6.1% average performance increase.



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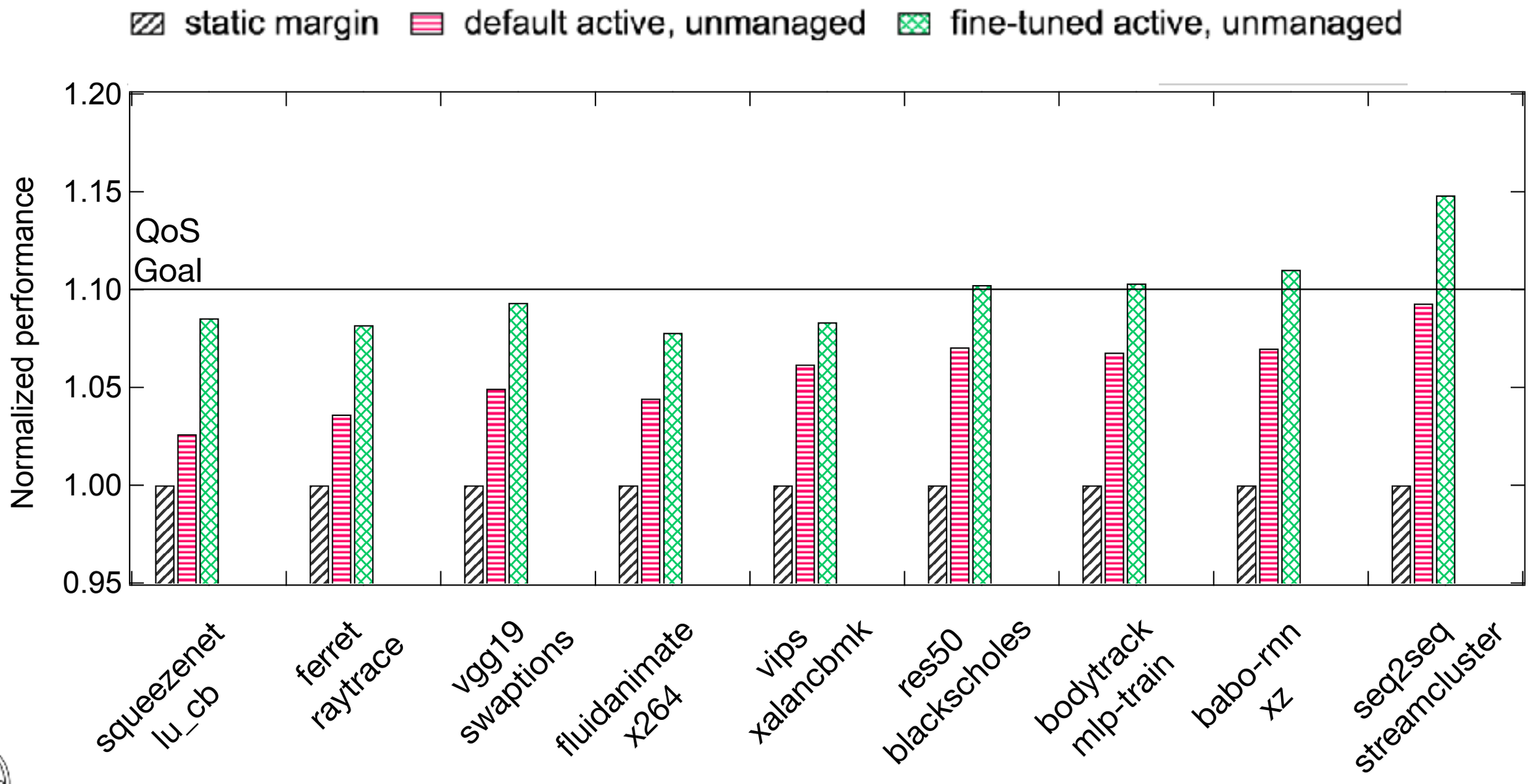
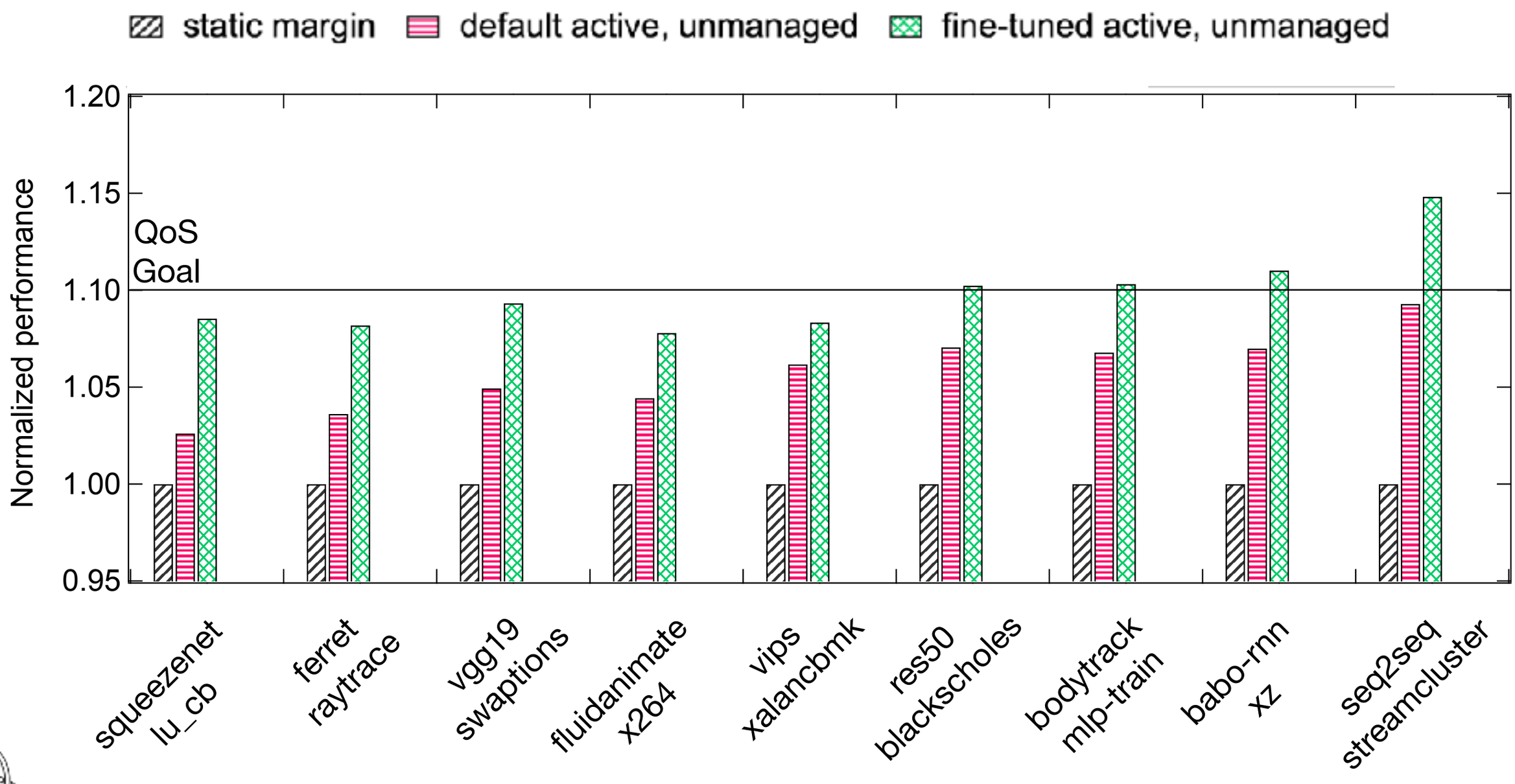


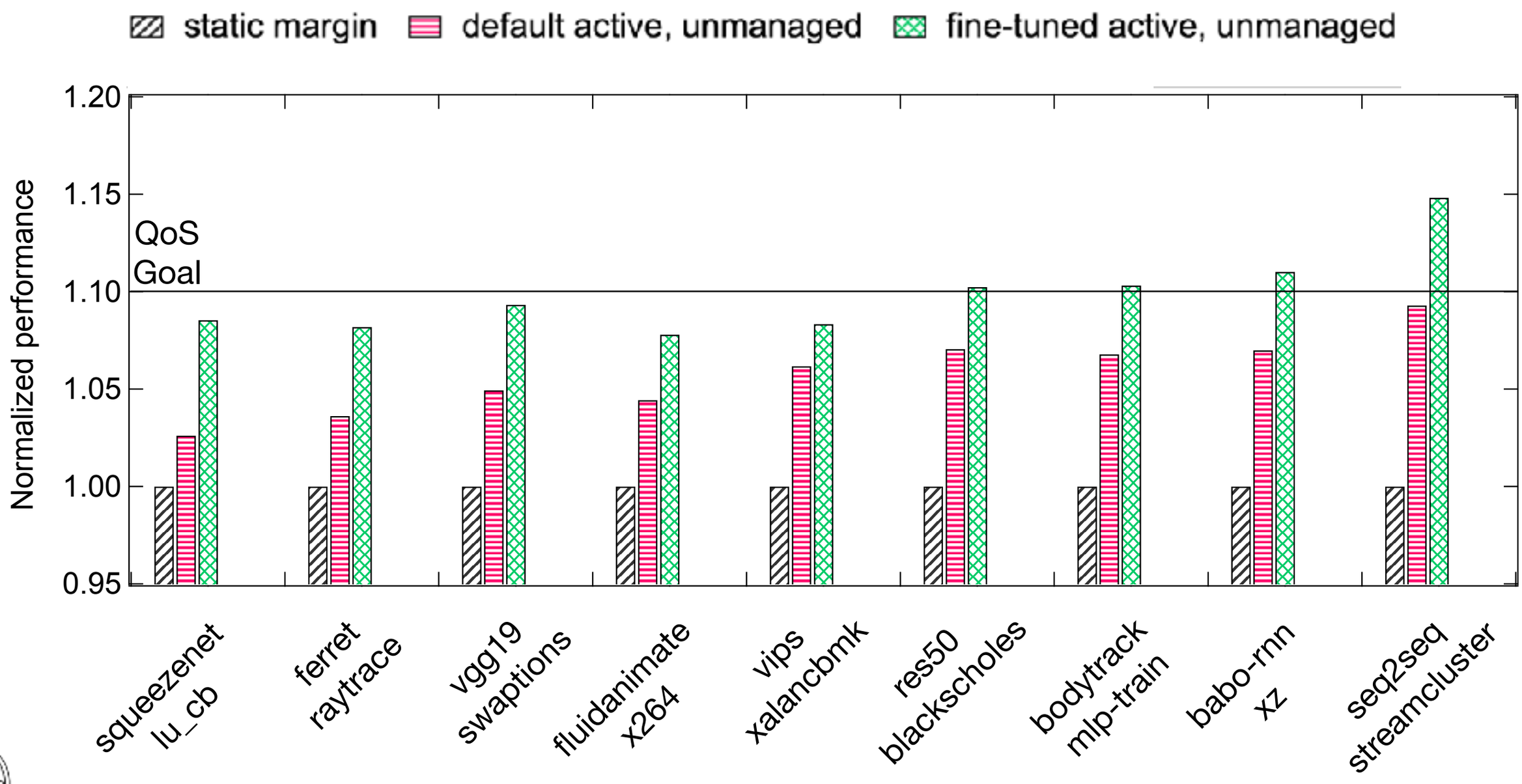
Performance Improvement

- Schedule to slow cores, with high power co-runner



Performance Improvement

- Schedule to slow cores, with high power co-runner
- 10.2% average performance increase



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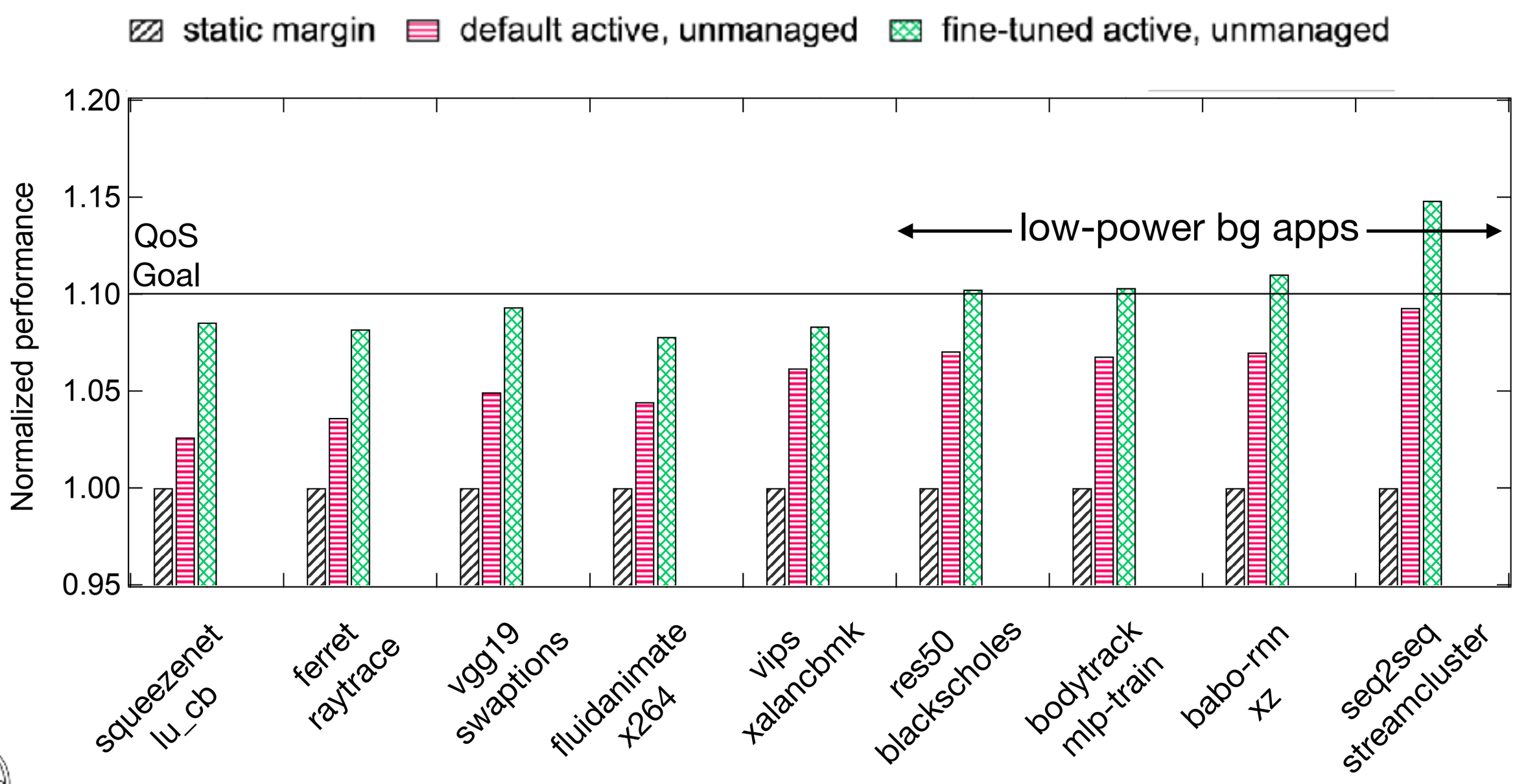
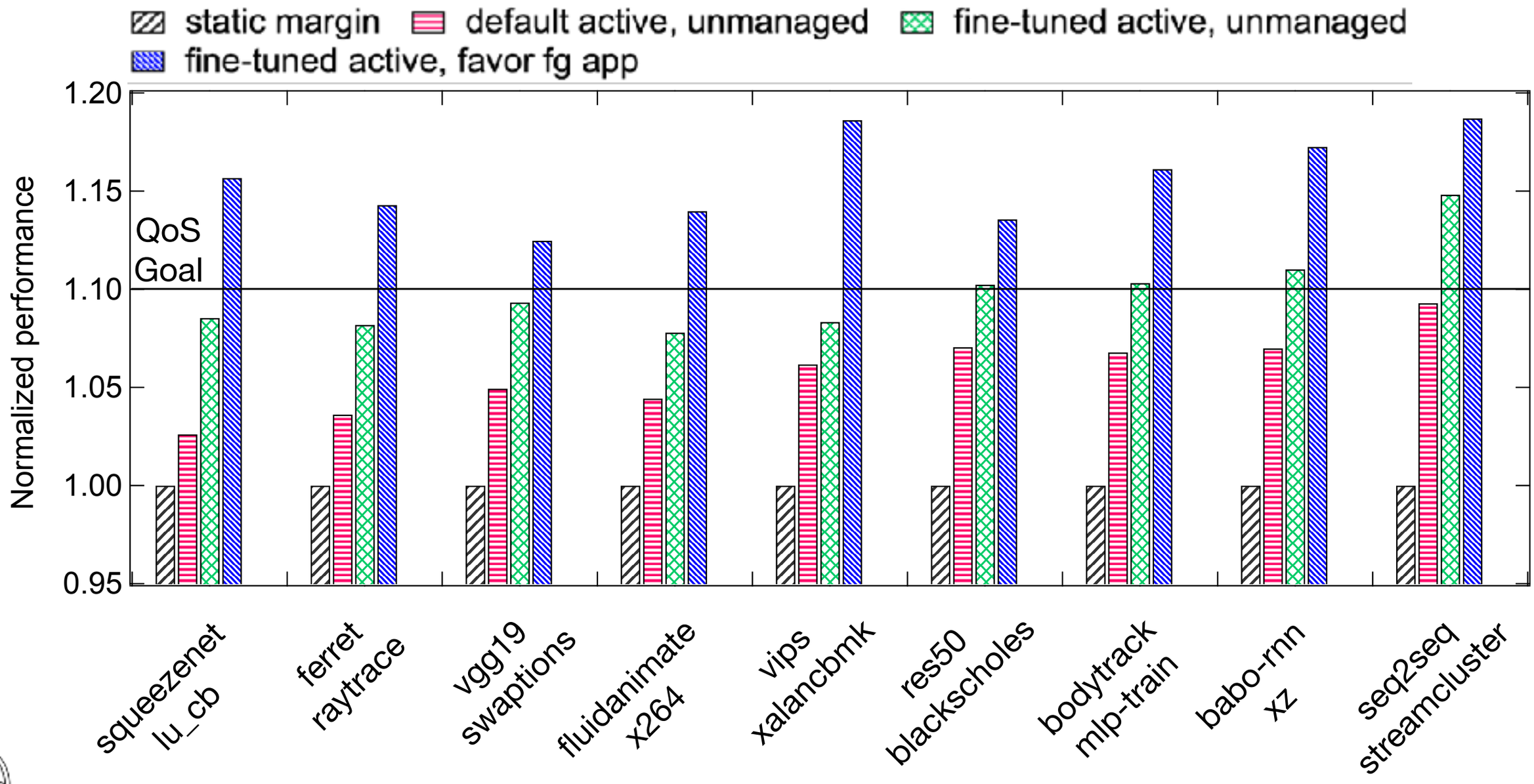
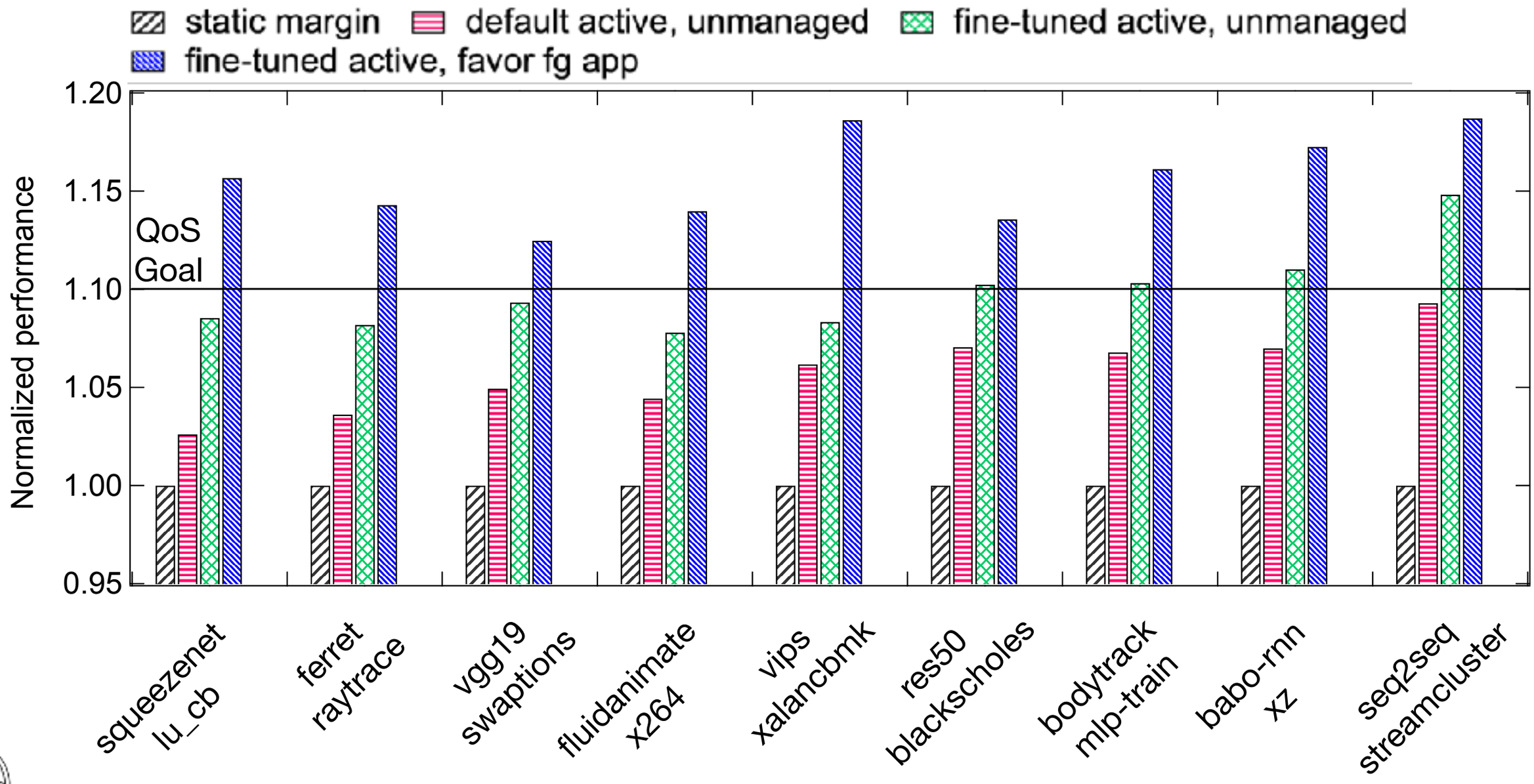


Performance Improvement



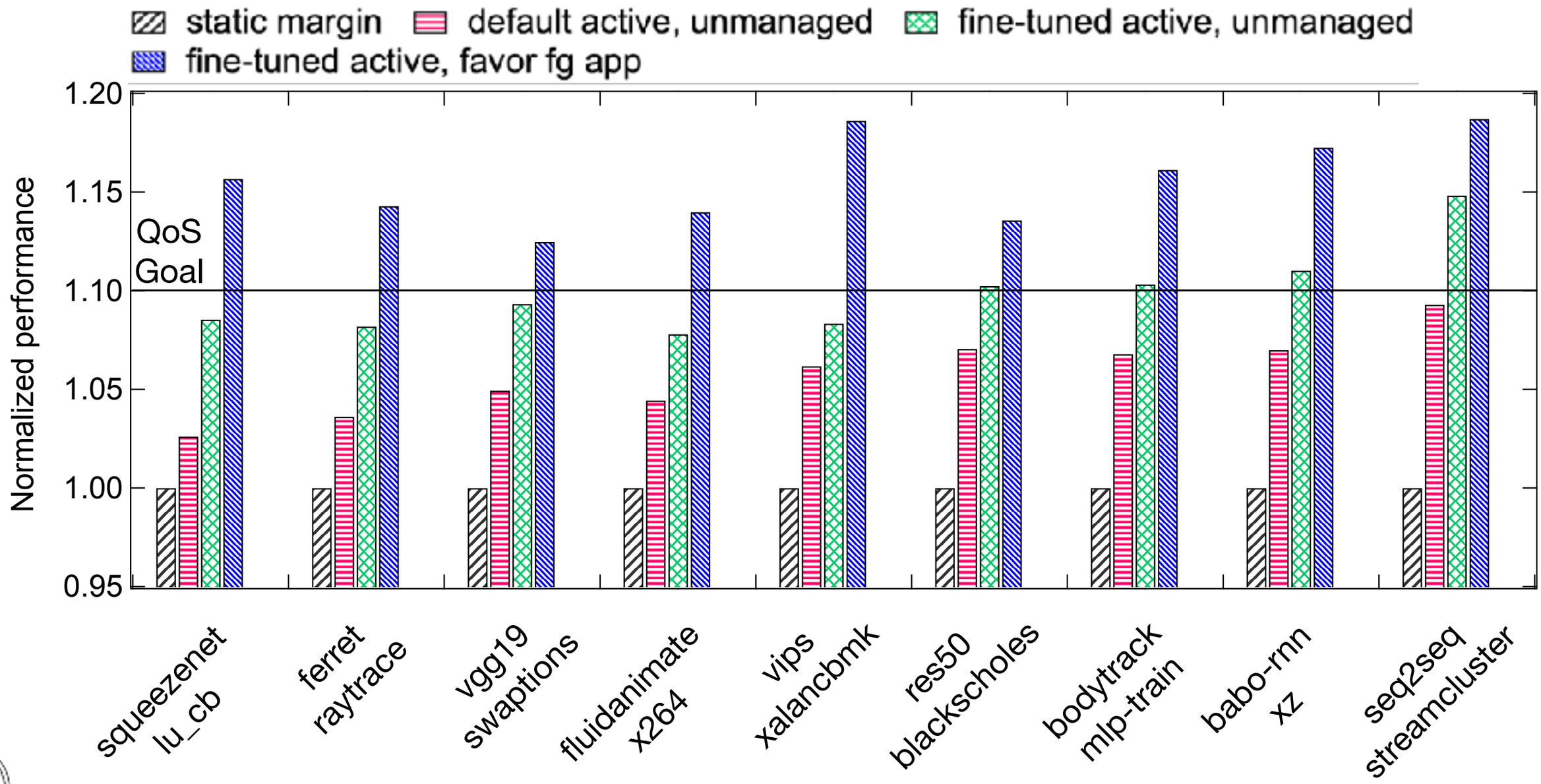
Performance Improvement

- Schedule to fast cores, and throttle co-runners to low p-states

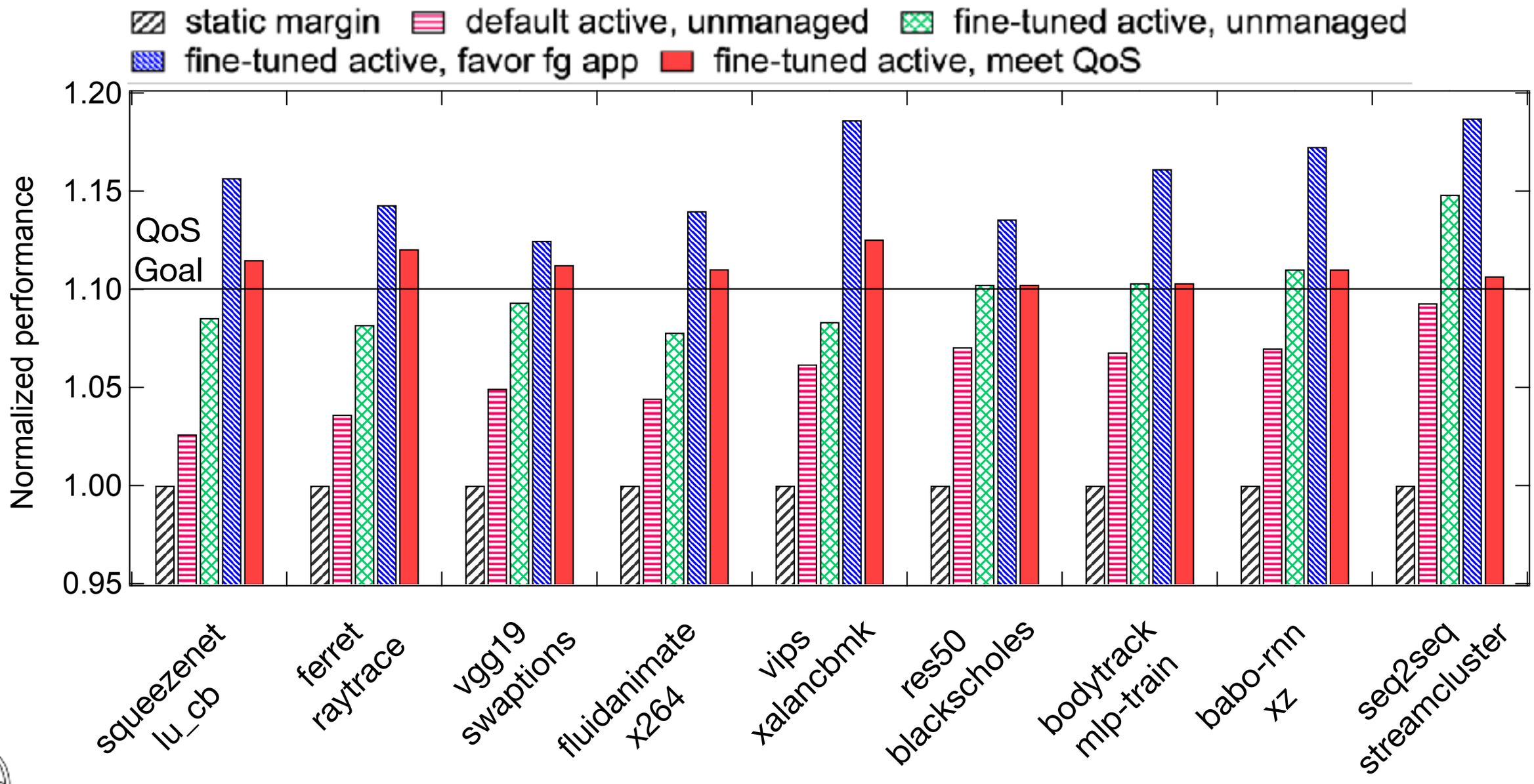


Performance Improvement

- Schedule to fast cores, and throttle co-runners to low p-states
- 15.2% average performance increase.

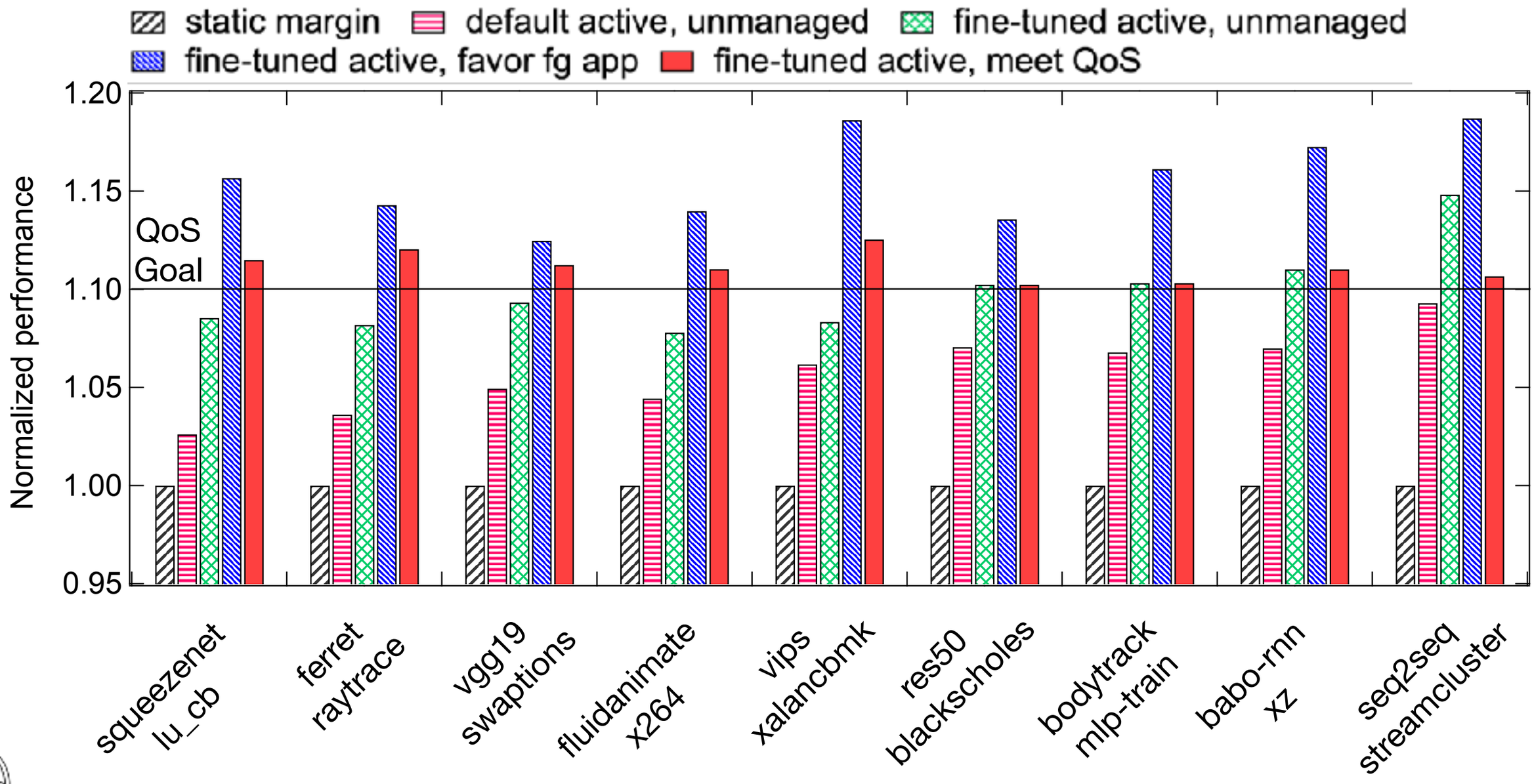


Performance Improvement



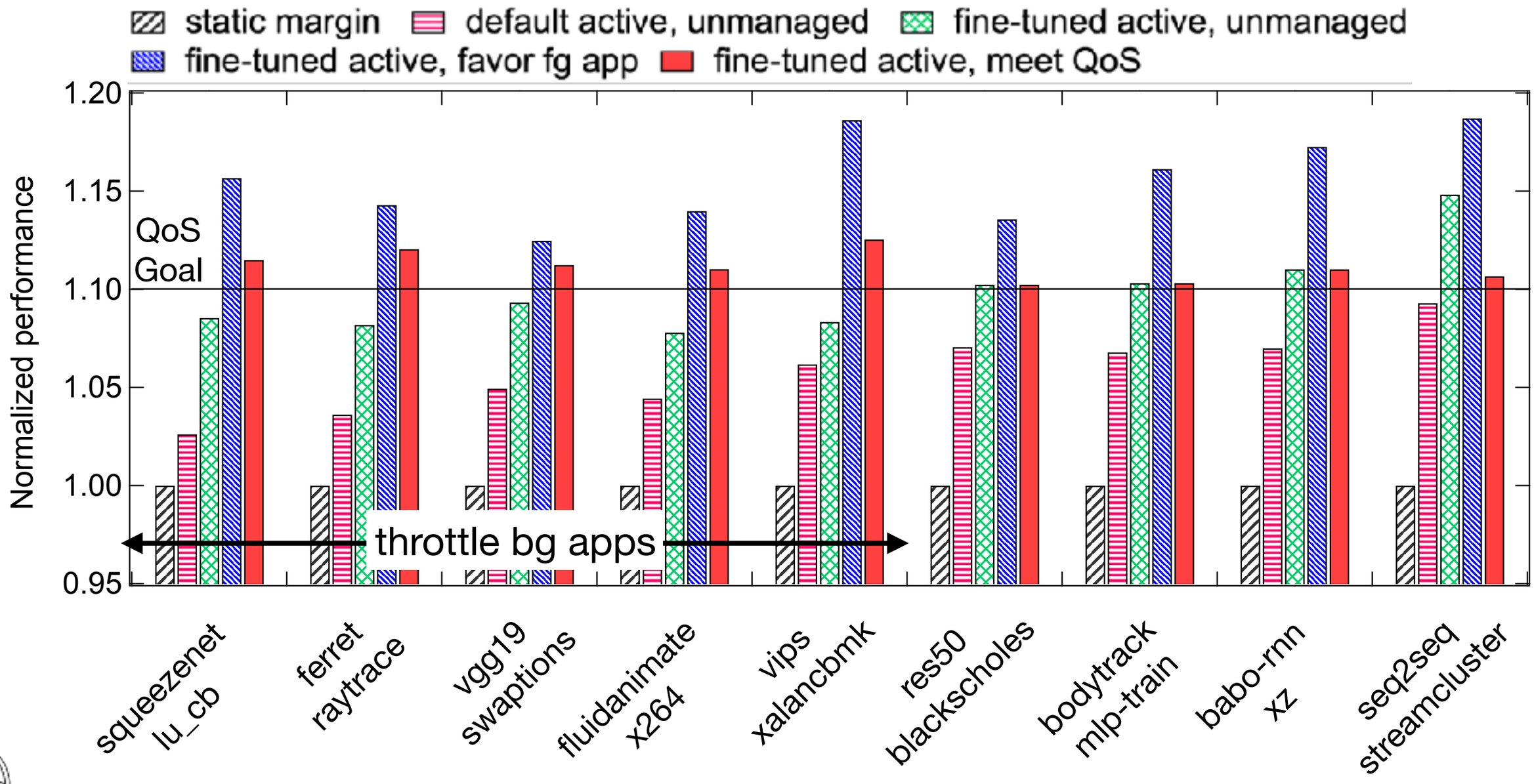
Performance Improvement

- Schedule to fast cores, and control co-runners' power



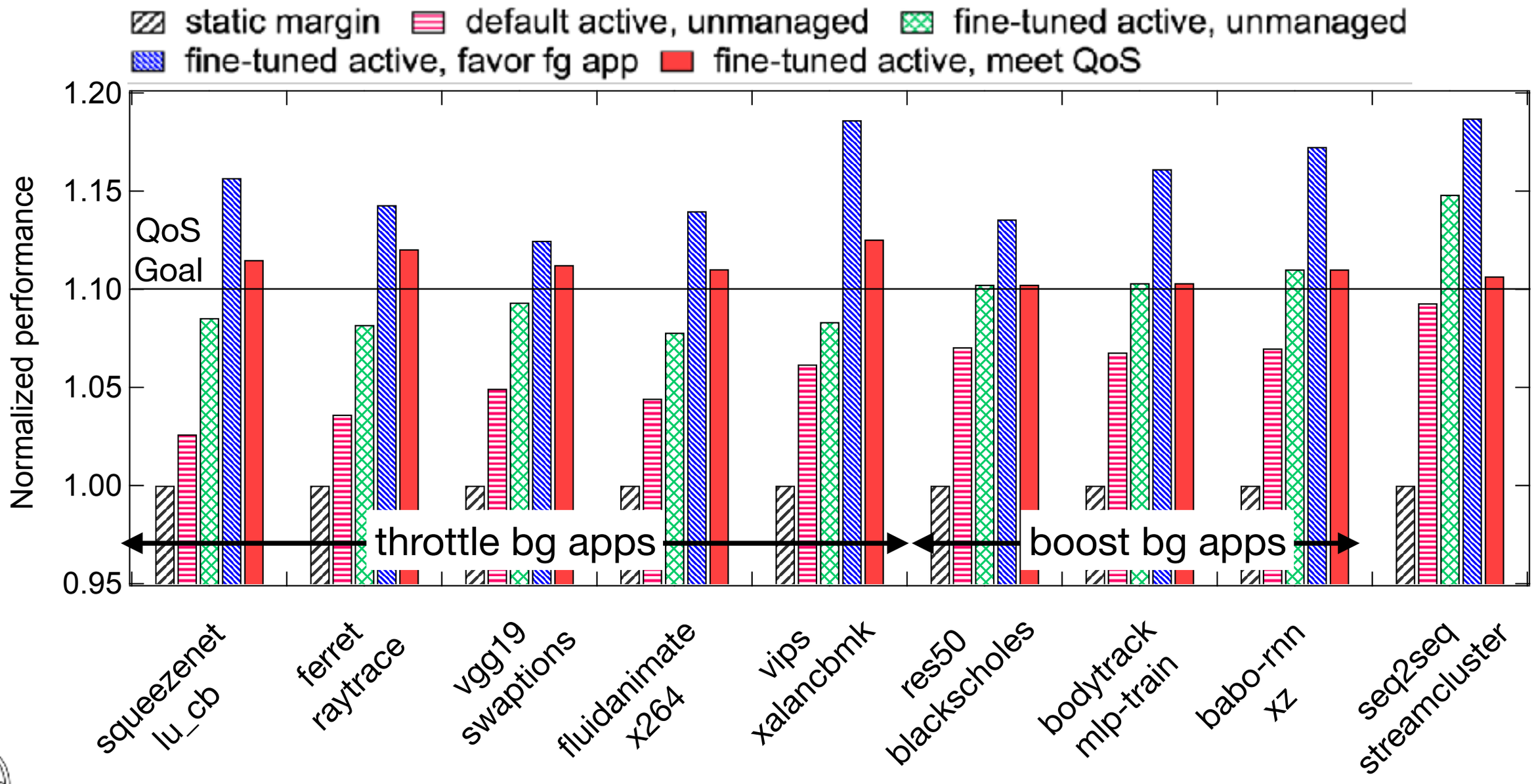
Performance Improvement

- Schedule to fast cores, and control co-runners' power



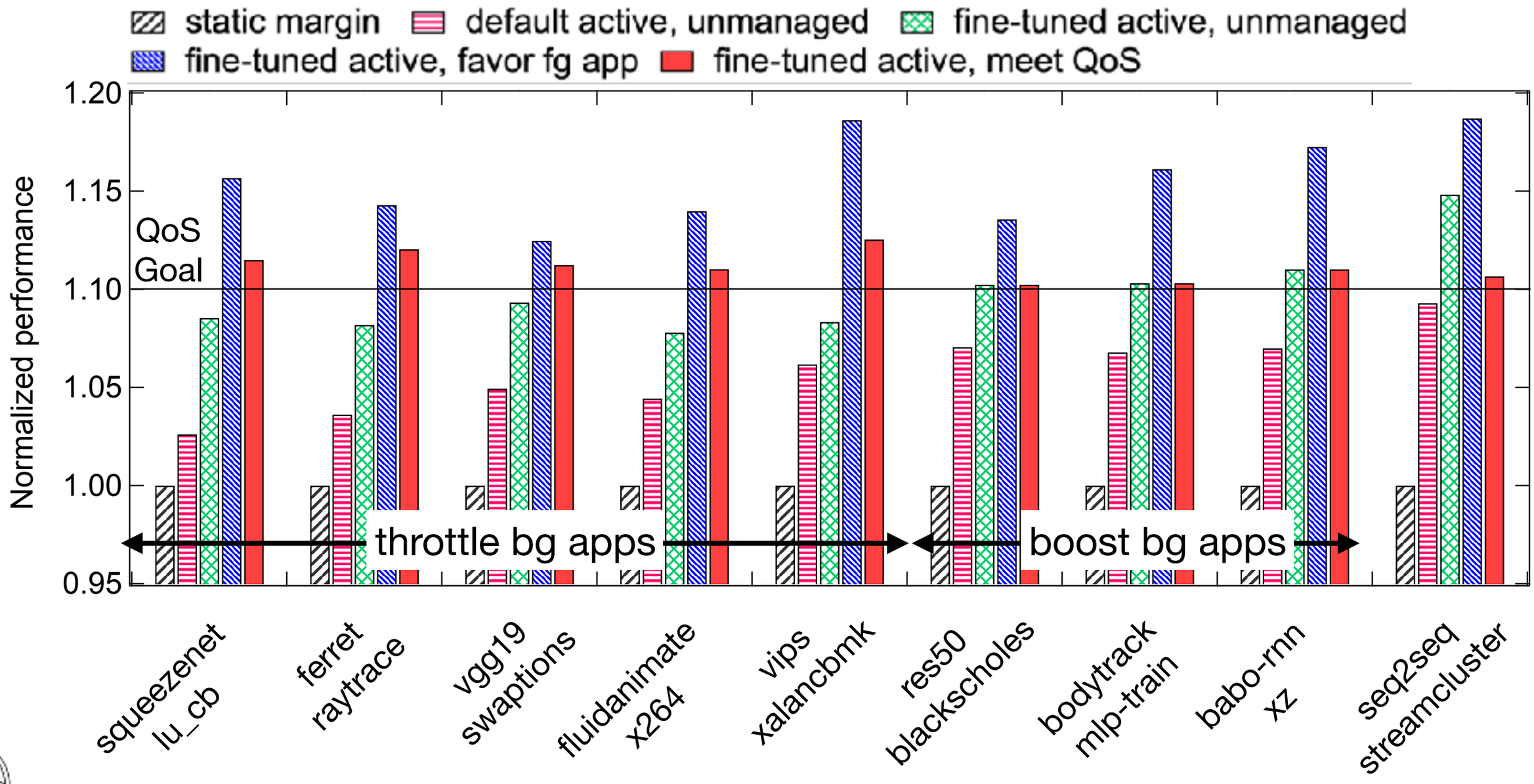
Performance Improvement

- Schedule to fast cores, and control co-runners' power



Performance Improvement

- Schedule to fast cores, and control co-runners' power
- Guaranteed 10% performance improvement.

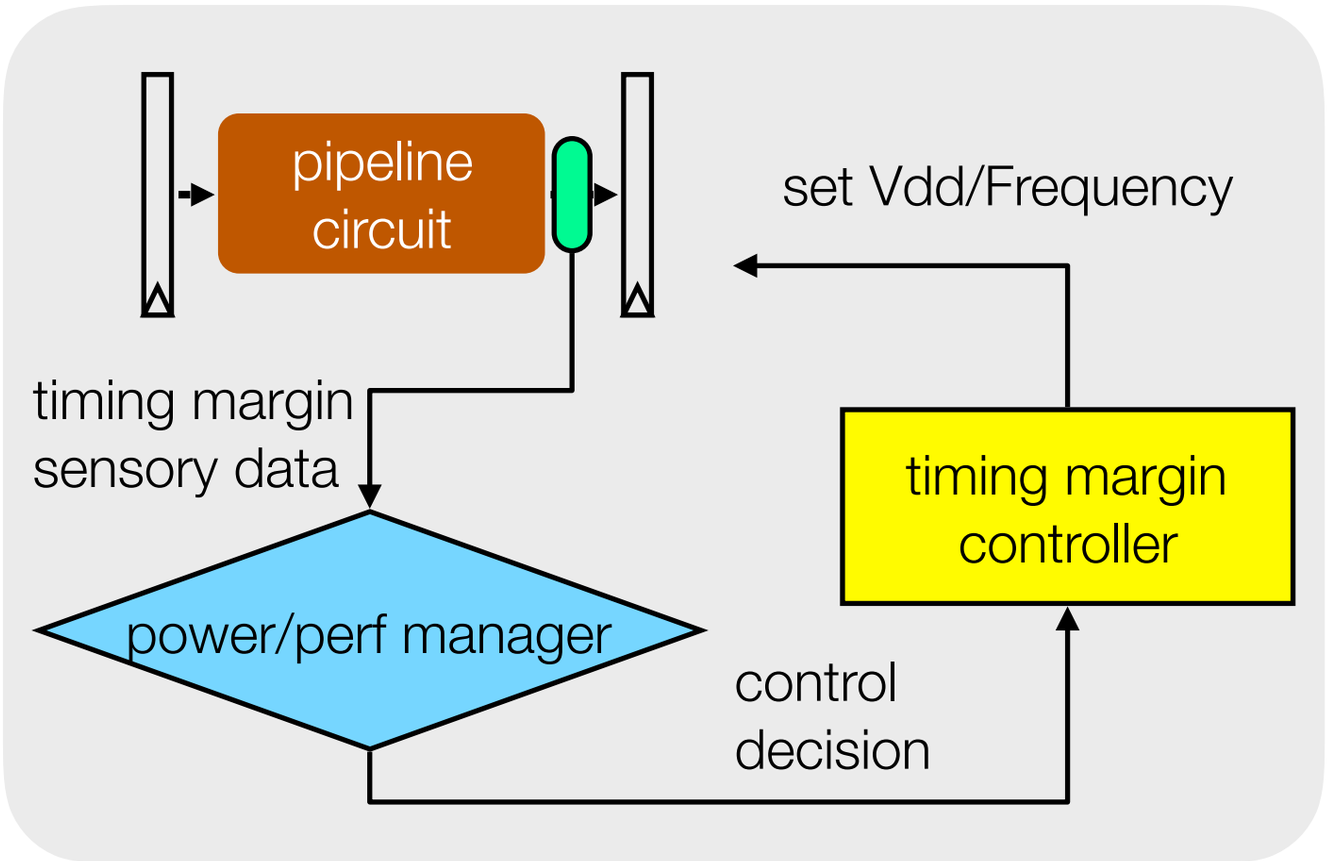


Managing Active Timing Margin

Applications

Software

Hardware

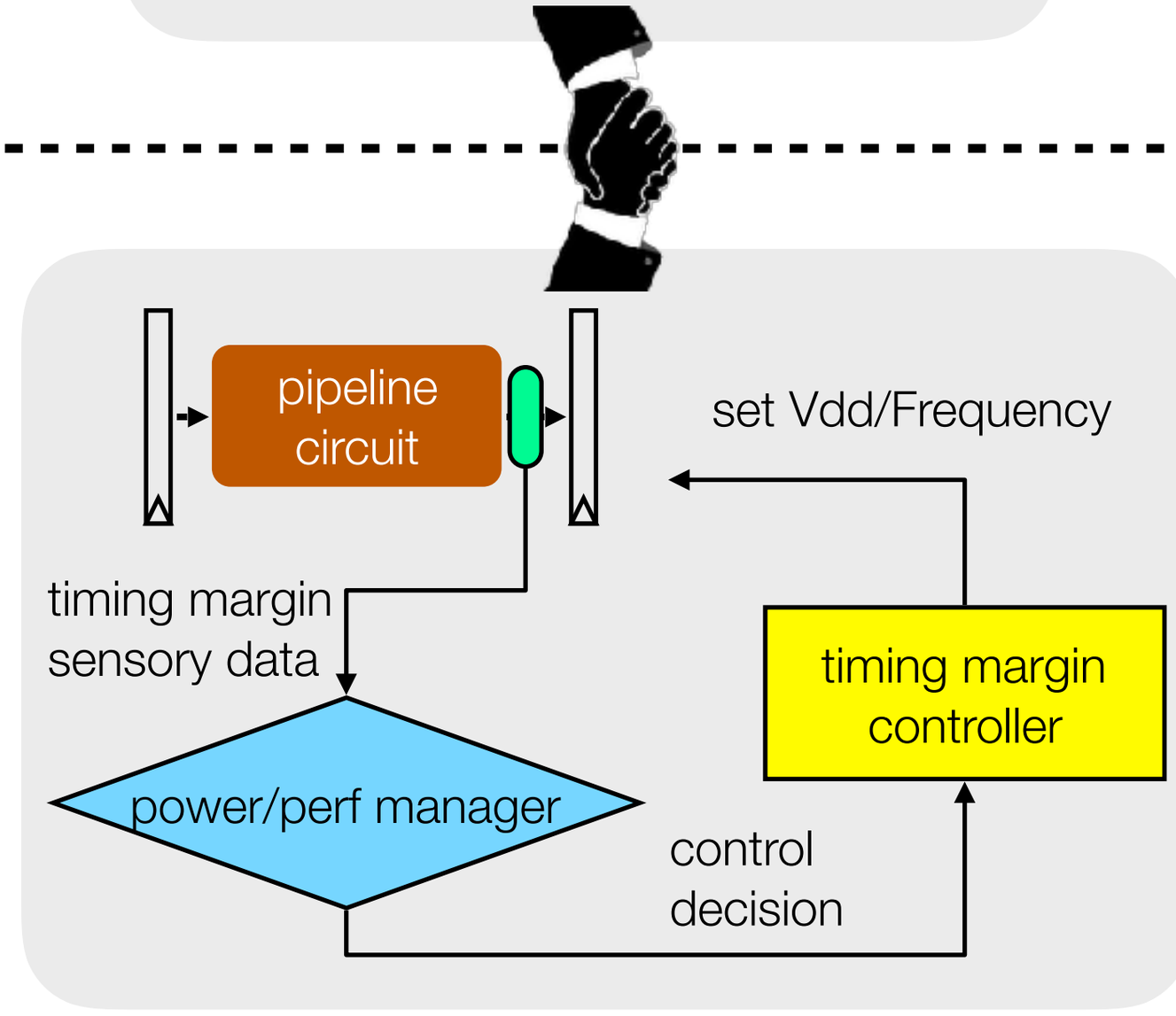


Managing Active Timing Margin - Bridging HW/SW

Applications

Software

Hardware



Backup

Active Management of Timing Guardband to Save Energy in POWER7*

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Robust power management in the IBM z13

A 22nm Dynamically Adaptive Clock Distribution for Voltage Droop Tolerance

8.5 **A 16nm Auto-Calibrating Dynamically Adaptive Clock Distribution for Maximizing Supply-Voltage-Droop Tolerance Across a Wide Operating Range**

margin for rising and falling input transitions to a positive value within a small TDE delay. The 3rd state inserts a positive timing margin into the DVM_{ROOT} by removing a programmable number of large TDEs so the ACD does not react to frequent small-magnitude V_{DD} variations. Finally, the FSM transitions back to the

16.4 **Adaptive Frequency and Biasing Techniques for Tolerance to Dynamic Temperature-Voltage Variations and Aging**

tion of the core when the TCP/IP header has finished processing and the core is idle. Both NMOS and PMOS body bias generators are implemented on the die and each includes a central bias generator (CBG) which is controlled by the DAB control, and many local bias

5.7 **A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep**

GRF bitcells to be connected to V_{BOOST} which acts as an always-on supply (Fig. 5.7.2). The bitcells are also disconnected from the WBLs. For storage of critical state distributed in the execution core, state-retention sequentials (Fig. 5.7.3) isolate the slave storage node during sleep and connect to an always-on "$V_{...}$"

5.6 **Adaptive Clocking System for Improved Power Efficiency in a 28nm x86-64 Microprocessor**

To create an instantly reduced clock frequency, a phase generator with a DLL is used to generate 20 phases of the PLL output clock. The DLL operates at a regulated voltage. To support finer stretch amounts, the 20 clock phases are

18.1 **Droop Mitigation using Critical-Path Sensors and an On-Chip Distributed Power Supply Estimation Engine in the z14™ Enterprise Processor**

in a single power-management unit and a global per-core throttling signal was sent to the targeted units for instruction throttling. In this design, each CPM still sends its output to the per-core power-management unit, but is also involved in a local loop. The local loop only uses a single CPM and a local copy of the power-management logic; it uses a process similar to an original loop, but with different filter, threshold, and slope parameters. Each local loop throttles a single unit in the core, but has a much faster response time. The local throttling signals are merged appropriately with the full core throttling loop signals to avoid excessive throttling.

The third new technique is to use CPM information from neighboring cores. Measurements of the previous generation modules revealed that power supply noise generated in one core propagates to neighboring cores approximately 5ns later [4]. CPM droop information can be sent to neighboring cores faster than

Christos Vezyrtzis[1], Thomas Strach[2], Pierce I-Jen Chuang[1], Preetham Lobo[3], Richard Rizzolo[4], Tobias Webel[2], Pawel Owczarczyk[4], Alper Buyuktosunoglu[1], Ramon Bertran[1], David Hui[4], Susan M. Eickhoff[4], Michael Floyd[5], Gerard Salem[6], Sean Carey[4], Stelios G. Tsapepas[4], Phillip J. Restle[1]

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▷ Active timing margin saves 10%~20% processor power

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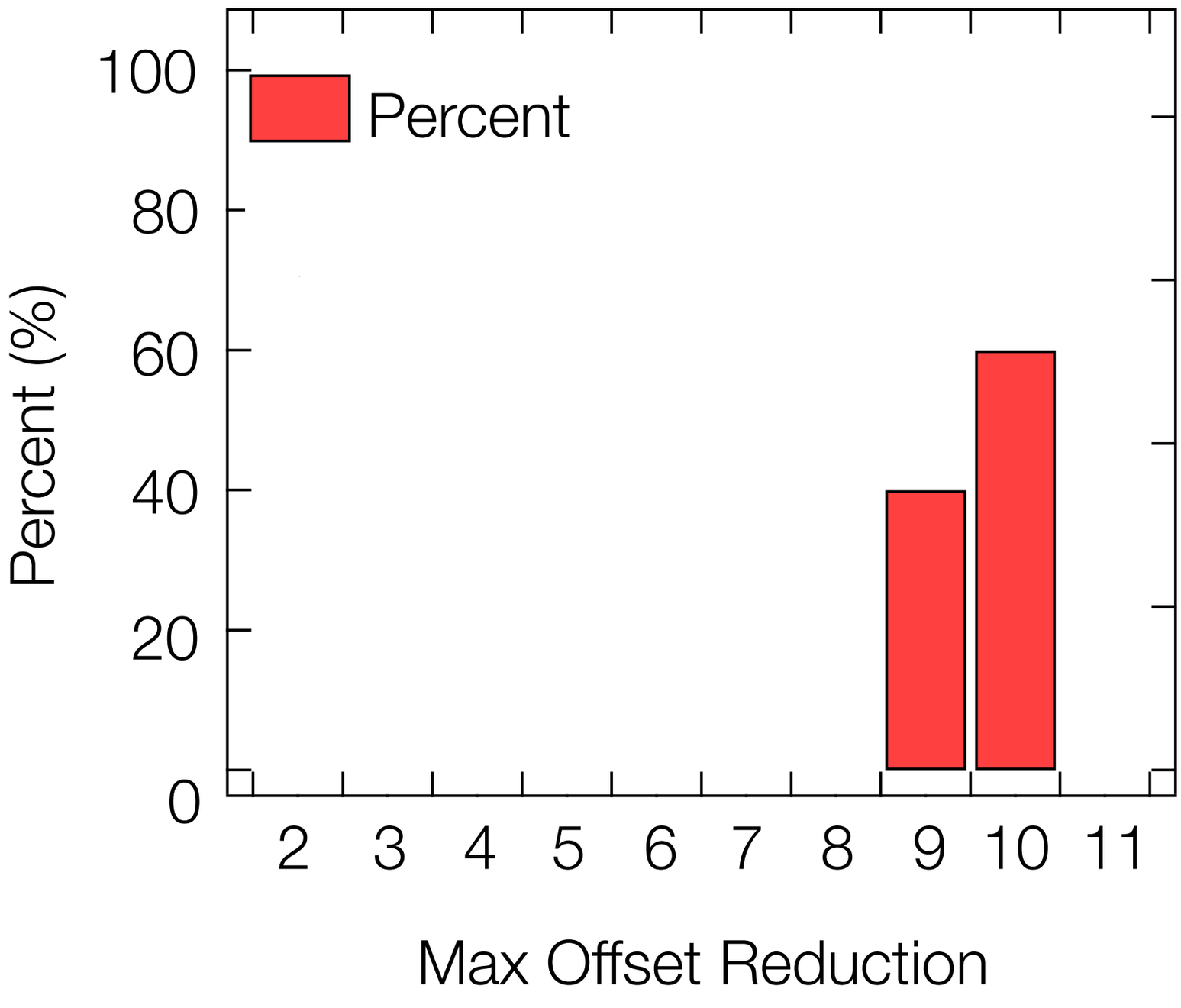
Fine-tuning Active Timing Margin: The Limits



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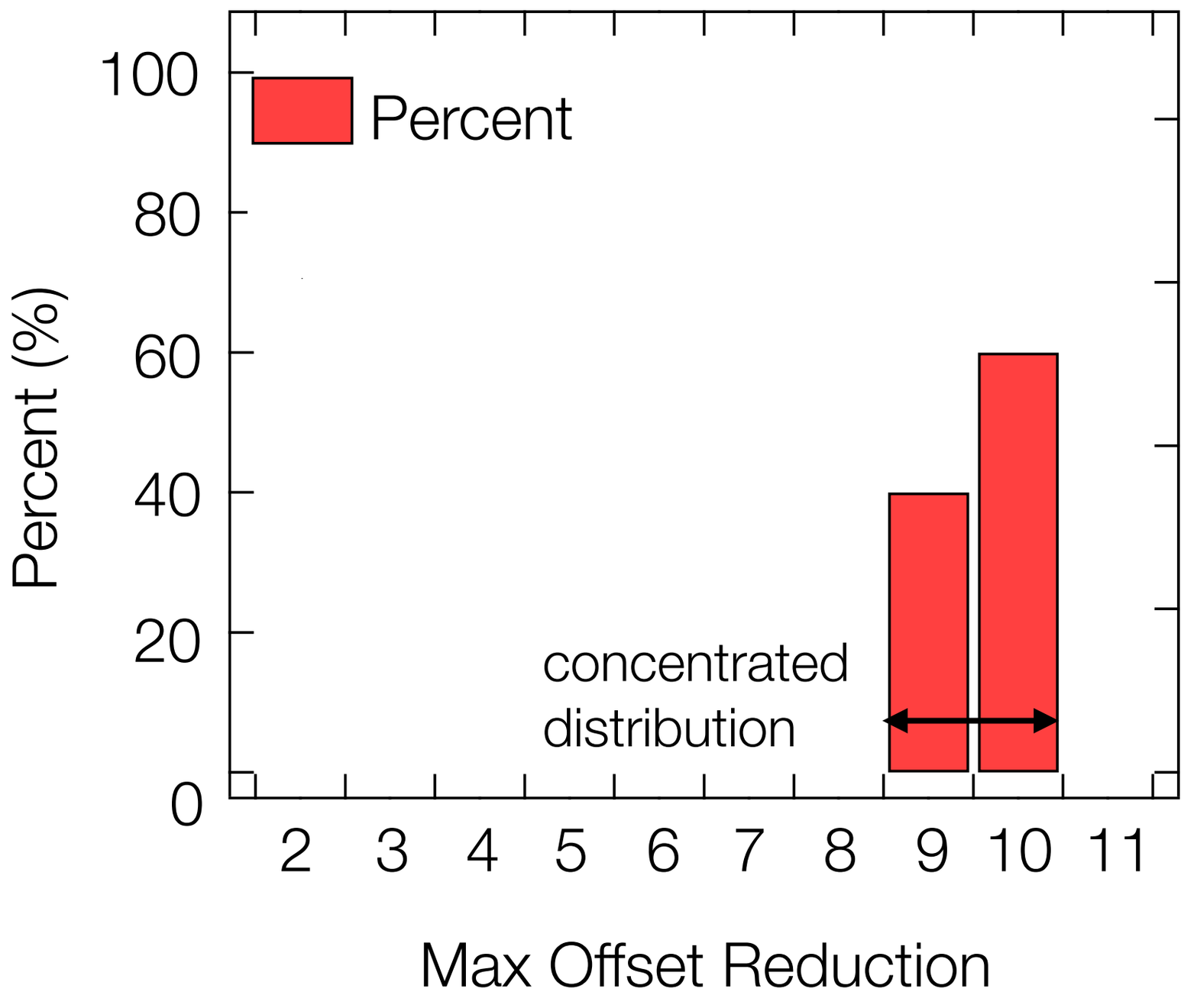

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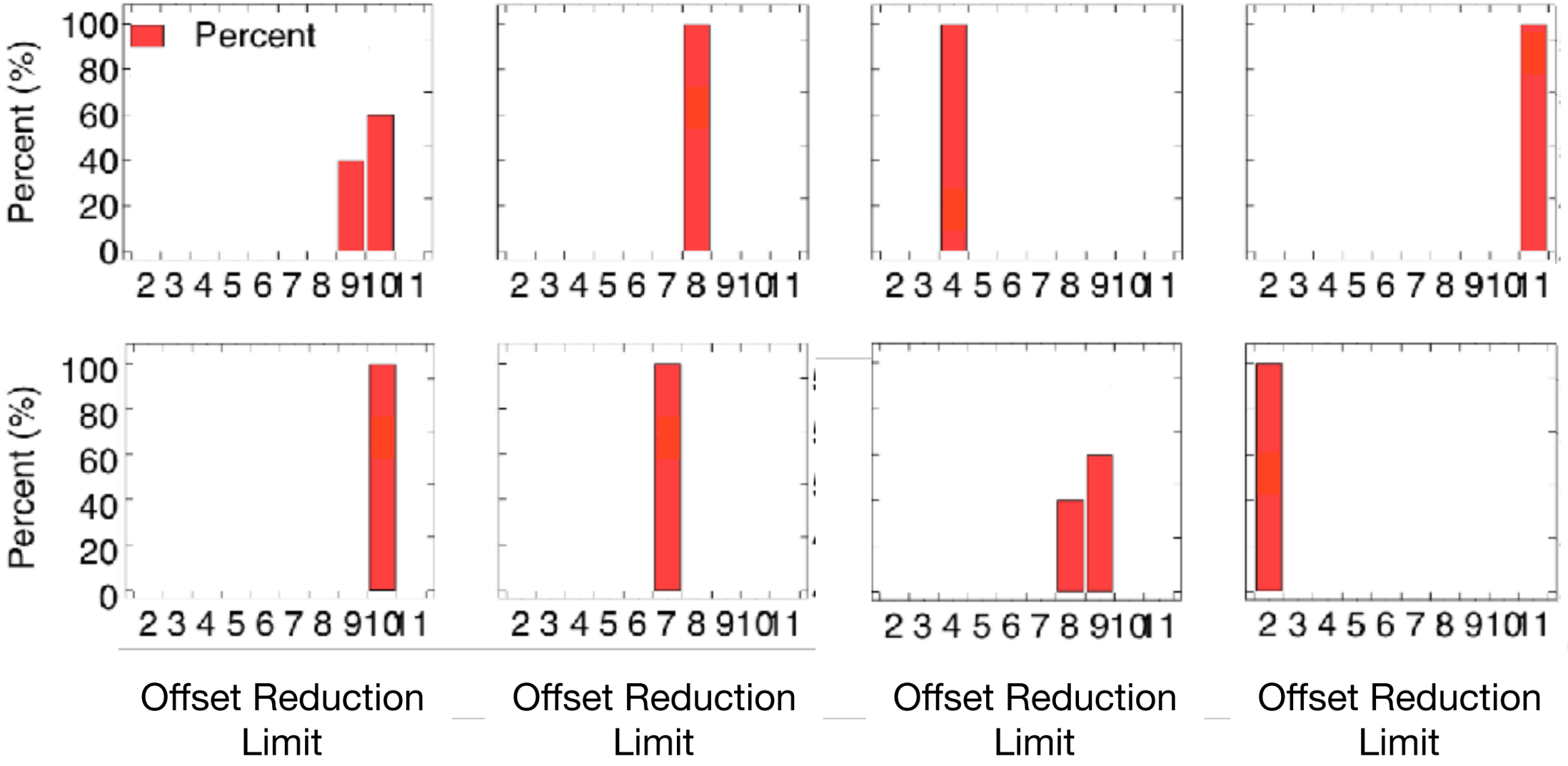

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