

# Matthew M. Ziegler

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<https://scholar.google.com/citations?user=1ds1ObgAAAAJ&hl=en>  
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<https://www.linkedin.com/in/matthew-m-ziegler>

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## RESEARCH INTERESTS

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VLSI design productivity, low power, CAD, artificial intelligence (AI), machine learning, nanoelectronics

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## FULL-TIME EMPLOYMENT

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**IBM T.J. Watson Research Center**  
PRINCIPAL RESEARCH STAFF MEMBER

**June 2018 - present**  
YORKTOWN HEIGHTS, NY

**IBM T.J. Watson Research Center**  
RESEARCH STAFF MEMBER

**June 2004 - 2018**  
YORKTOWN HEIGHTS, NY

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## EDUCATION

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**PhD in Electrical Engineering**  
UNIVERSITY OF VIRGINIA

**2000-2004**  
CHARLOTTESVILLE, VA

*Department:* Electrical and Computer Engineering  
*Dissertation:* “Regularly structured design for coping with nanoscale integration complexity”  
*Advisor:* Prof. Mircea Stan  
*Teaching Assistant:* VLSI Design, Advanced Digital Design  
*Research Assistant:* Topics: VLSI for nanoelectronics, High-performance arithmetic circuits

**B.S.E.E. degree**  
UNIVERSITY OF VIRGINIA

**1996-2000**  
CHARLOTTESVILLE, VA

*Major:* Electrical Engineering  
*Minor:* Computer Science  
*Thesis Topic:* “VLIW Architecture and VLSI Implementation for Video Signal Processors”  
*Activities:* SRC Copper IC contest, Intramural Soccer, Martial Arts

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## INTERNSHIPS

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**MITRE Corporation**  
NANOSYSTEMS GROUP MEMBER

**June 2001 – June 2004**  
MCLEAN, VA

Research on the topics of VLSI design, circuit simulation and CAD for molecular nanoelectronics.  
Funded by the DARPA Moletronics and MolApps programs.

**Annapolis Micro Systems, Inc.**  
ASIC DESIGN GROUP MEMBER

**June - August 2000**  
ANNAPOLIS, MD

Worked primary in simulation, layout and verification for mixed-signal CMOS circuits, including: phase-locked loops, oscillators, and amplifiers. Also modeled circuits via VHDL.

**Princeton University**

SUMMER RESEARCH STUDENT

Conducted research for the design of a programmable video signal processor. Work included: architecture, schematics, simulations, and layouts for a proposed single chip video processor.

**June - August 1999**

PRINCETON, NJ

**Thomson Consumer Electronics**

RESEARCH ASSISTANT

Assisted in researching experimental screening technology for television tubes.

**May – August 1998**

LANCASTER, PA

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**AWARDS AND DISTINCTIONS**

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**IBM Research Technical Accomplishment Awards**

16 Total Awards (10 A-Level (A), 5 Outstanding (O), 1 Extraordinary (E))

2019 (A): Digital AI Hardware Accelerator Research and Commercialization

2019 (A): Resilient, Low Power Acceleration Technology

2018 (O): Automated Parameter Tuning for Server Macro Optimization

2018 (A): Impact of Approximate Computing on AI Hardware Acceleration Innovations

2017 (A): eFinale Power Reduction for Server Macros

2016 (O): Contributions to POWER8 Processor and Memory I/O Design

2015 (O): Z Systems Research

2014 (A): SynTunSys: A System for Automatically Optimizing Macro Build Parameters

2014 (A): Contributions to POWER8 Processor and Memory I/O Design

2013 (E): Blue Gene as a Product

2013 (A): Contributions to POWER7+ Processor Chip Design

2012 (O): POWER7 Microprocessor and Memory Hub Chip Design Contributions

2010 (A): Power7 Microprocessor Chip Design

2009 (O): Large Block and Structured Synthesis for Server Design Productivity

2008 (A): Large Block Synthesis and Structured Synthesis for Server Design Productivity

2005 (A): Firm IP (FIP) Integrated Circuit Layout Assembly Toolkit

**IBM Academy of Technology Member (Elected in 2018)****SRC Mahboob Khan Outstanding Industry Liaison Award 2018**

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**EXTERNAL & IBM PROFESSIONAL ACTIVITIES**

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**IEEE / ACM Conference & Journal Activities**

ISLPED – General Co-Chair, 2019

ISLPED – TPC Co-Chair, 2018

ISLPED – TPC Member, 2005 - present

DAC TPC Member, 2020 - present

GLSVLSI TPC Member, 2017 - 2019

IBM IEEE CAS/EDS 3st AI Compute Symposium – TPC Co-Chair, 2020

IBM IEEE CAS/EDS 2st AI Compute Symposium – TPC Co-Chair, 2019

IBM IEEE CAS/EDS 1st AI Compute Symposium – TPC Co-Chair, 2018

IBM IEEE CAS/EDS Emerging Technology Symposium – TPC Co-Chair, 2017

IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) Senior Editor, 2020 - present

### **SRC (Semiconductor Research Corporation) Activities**

SRC Mahboob Khan Outstanding Industry Liaison Award 2018

SRC AI Hardware Technical Advisory Board Member Alternate 2019 – present

SRC EP3C / E2CDA Program Co-chair 2014 – 2019

SRC Advanced Connectivity Program Co-chair 2013 – 2014

The SRC (Semiconductor Research Corporation) Advanced Connectivity & EP3C (Efficiency and Performance for Connectivity Constrained Computing) programs targeting fundamental research that will identify disruptive solutions designed to minimize the energy cost of moving data.

### **Professional Society Memberships**

IEEE Member, IEEE CAS Society Member, IEEE SSCS Society Member

### **IBM Society Activities**

IBM Academy of Technology Member (Elected in 2018)

IBM Research Computer Systems Design PIC Co-Chair 2017 – present

IBM Research VLSI PIC Chair 2013 - 2017

IBM PICs (professional interest communities) are responsible for fostering research collaboration between IBM and external researchers through activities such as: external speaker seminars, financial sponsorship of external conferences, organizing internal and external workshops, university visits, etc.

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### **ISSUED PATENTS (20)**

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“Optimizing the layout of circuits based on multiple design constraints”

RL Franch, GD Gristede, MM Ziegler

US Patent 10,296,692, 2019/5/21

“Resonant virtual supply booster for synchronous digital circuits having a predictable evaluate time”

RV Joshi, MM Ziegler

US Patent 10,263,519, 2019/4/16

"Scheduling simultaneous optimization of multiple very-large-scale-integration designs"

H-Y Liu, MM Ziegler

US Patent 9,600,623, 2018/9/24

"Enhanced parameter tuning for very-large-scale integration synthesis"

H-Y Liu, MM Ziegler

US Patent 10,002,221, 2018/6/18

"Enhanced parameter tuning for very-large-scale integration synthesis"

H-Y Liu, MM Ziegler

US Patent 9,934,344, 2018/4/2

"Synthesis tuning system for VLSI design optimization"

GD Gristede, MM Ziegler

US Patent 9,910,949, 2018/3/6

"Intra-run design decision process for circuit synthesis"

CJ Berry, L Reddy, S Saha, MM Ziegler

US Patent 9,703,920, 2017/7/11

"Intra-run design decision process for circuit synthesis"

CJ Berry, L Reddy, S Saha, MM Ziegler

US Patent 9,690,900, 2017/6/27

"Resonant virtual supply booster for synchronous digital circuits having a predictable evaluate time"

RV Joshi, MM Ziegler

US Patent 9,660,530, 2017/5/23

"Enhanced parameter tuning for very-large-scale integration synthesis"

H-Y Liu, MM Ziegler

US Patent 9,619,602, 2017/4/11

"Scheduling simultaneous optimization of multiple very-large-scale-integration designs"

H-Y Liu, MM Ziegler

US Patent 9,600,623, 2017/3/20

"Enhanced parameter tuning for very-large-scale integration synthesis"

H-Y Liu, MM Ziegler

US Patent 9,582,627, 2017/2/28

"Synthesis tuning system for VLSI design optimization"

GD Gristede, MM Ziegler

US Patent 9,529,951, 2016/12/26

"Graphical method and product to assign physical attributes to entities in a high level descriptive language used for vlsi chip design"

John T. Badar, David W. Lewis, Michael H. Wood, Matthew M. Ziegler

US Patent 8,954,914, 2015/2/10

"Specifying circuit level connectivity during circuit design synthesis"

Michael D Amundson, Dorothy Kucar, Ruchir Puri, Chin Ngai Sze, Matthew M Ziegler

US Patent 8,839,162, 2014/9/16

"Relative ordering circuit synthesis"

Minsik Cho, Ruchir Puri, Haoxing Ren, Xiaoping Tang, Hua Xiang, Matthew Mantell Ziegler

US Patent 8,756,541, 2014/6/17

"Network flow based datapath bit slicing"

H Xiang, M Cho, H Ren, MM Ziegler, R Puri

US Patent 8,566,761, 2013/10/22

Soft hierarchy-based physical synthesis for large-scale, high-performance circuits

M Cho, AW Ng, R Puri, H Ren, H Xiang, MM Ziegler

US Patent 8,516,412, 2013/8/20

"Structured latch and local-clock-buffer planning"

M Cho, R Puri, H Ren, H Xiang, MM Ziegler

US Patent 8,495,552, 2013/7/23

"Converged large block and structured synthesis for high performance microprocessor designs"

Minsik Cho, Victor N. Kravets, Smita Krishnaswamy, Dorothy Kucar, Jagannathan Narasimhan, Ruchir Puri, Haifeng Qian, Haoxing Ren, Chin Ngai Sze, Louise H. Trevillyan, Hua Xiang, Matthew M. Ziegler

US Patent 8,271,920, 2012/9/18

### Conference Publications (40)

**Notable Conference Publications: ISSCC (2), VLSI (4), CICC (3), DAC (1), ICCAD (2), DATE (2), ISPD (1), ISLPED (5), HPCA (1), ISQED (1), GLSVLSI (1), Invited papers (4)**

Jinwook Oh, Sae Kyu Lee, Mingu Kang, Matthew Ziegler, Joel Silberman, Ankur Agrawal, Swagath Venkataramani, Bruce Fleischer, Michael Guillorn, Jungwook Choi, Wei Wang, Silvia Mueller, Shimon Ben-Yehuda, James Bonanno, Nianzheng Cao, Robert Casatuta, Chia-Yu Chen, Matt Cohen, Ophir Erez, Thomas Fox, George Gristede, Howard Haynie, Vicktoria Ivanov, Siyu Koswatta, Shih-Hsien Lo, Martin Lutz, Gary Maier, Alex Mesh, Yevgeny Nustov, Scot Rider, Marcel Schaal, Michael Scheuermann, Xiao Sun, Naigang Wang, Fanchieh Yee, Ching Zhou, Vinay Shah, Brian Curran, Vijayalakshmi Srinivasan, Pong-Fei Lu, Sunil Shukla, Kailash Gopalakrishnan, Leland Chang, "A 3.0 TFLOPS 0.62 V Scalable Processor Core for High Compute Utilization AI Training and Inference," VLSI Circuit Symposium (VLSI), June 2020.

Rajiv V Joshi, Matthew M Ziegler, "Low Power Design from Moore to AI for nm Era," International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), 2019 (**Invited**).

J. Kwon, M. M. Ziegler, L. P. Carloni, "A Learning-Based Recommender System for Autotuning Design Flows of Industrial High-Performance Processors," Design Automation Conference (DAC), 2019.

Nandhini Chandramoorthy, Karthik Swaminathan, Martin Cochet, Schuyler Eldridge, Arun Paidimarri, Rajiv Joshi, Matthew Ziegler, Alper Buyuktosunoglu, and Pradip Bose, "Resilient Low Voltage Acceleration for High Energy Efficiency," International Symposium on High-Performance Computer Architecture (HPCA), 2019.

Vijayalakshmi Srinivasan, Bruce Fleischer, Sunil Shukla, Matthew Ziegler, Joel Silberman, Jinwook Oh, Jungwook Choi, Silvia Mueller, Ankur Agrawal, Tina Babinsky, Nianzheng Cao, Chia-Yu Chen, Pierce Chuang, Thomas Fox, George Gristede, Michael Guillorn, Howard Haynie, Michael Klaiber, Dongsoo Lee, Shih-Hsien Lo, Gary Maier, Michael Scheuermann, Swagath Venkataramani, Christos Vezyrtzis, Naigang Wang, Fanchieh Yee, Ching Zhou, Pong-Fei Lu, Brian Curran, Leland Chang, Kailash Gopalakrishnan "Across the Stack Opportunities for Deep Learning Acceleration," International Symposium Low Power Electronics and Design (ISLPED), 2018 (**Invited**).

Bruce Fleischer, Sunil Shukla, Matthew Ziegler, Joel Silberman, Jinwook Oh, Vijayalakshmi Srinivasan, Jungwook Choi, Silvia Mueller, Ankur Agrawal, Tina Babinsky, Nianzheng Cao, Chia-Yu Chen, Pierce Chuang, Thomas Fox, George Gristede, Michael Guillorn, Howard Haynie, Michael Klaiber, Dongsoo Lee, Shih-Hsien Lo, Gary Maier, Michael Scheuermann, Swagath Venkataramani, Christos Vezyrtzis, Naigang Wang, Fanchieh Yee, Ching Zhou, Pong-Fei Lu, Brian Curran, Lel Chang, Kailash Gopalakrishnan, "A Scalable Multi-TeraOPS Deep Learning Processor Core for AI Training and Inference," VLSI Circuit Symposium (VLSI), June 2018.

RV Joshi, MM Ziegler, K Swaminathan, N Chandramoorthy, "Cascaded and resonant SRAM supply boosting for ultra-low voltage cognitive IoT applications," Custom Integrated Circuits Conference (CICC), 2018.

Ramon Bertran, Pradip Bose, David Brooks, Jeff Burns, Alper Buyuktosunoglu, Nandhini Chandramoorthy, Eric Cheng, Martin Cochet, Schuyler Eldridge, Daniel Friedman, Hans Jacobson, Rajiv Joshi, Subhasish Mitra, Robert Montoye, Arun Paidimarri, Pritish Parida, Kevin Skadron, Mircea Stan, Karthik Swaminathan, Augusto Vega, Swagath Venkataramani, Christos Vezyrtzis, Gu-Yeon Wei, John-David Wellman, Matthew Ziegler, "Very Low Voltage (VLV) Design," International Conference on Computer Design (ICCD), 2017.

RV Joshi, MM Ziegler, "Programmable supply boosting techniques for near threshold and wide operating voltage SRAM," Custom Integrated Circuits Conference (CICC), 2017.

Matthew M Ziegler, Hung-Yi Liu, Luca P Carloni, "Scalable Auto-Tuning of Synthesis Parameters for Optimizing High-Performance Processors," International Symposium Low Power Electronics and Design (ISLPED), 2016.

Matthew M Ziegler, Hung-Yi Liu, George Gristede, Bruce Owens, Ricardo Nigaglioni, Luca P Carloni, "A synthesis-parameter tuning system for autonomous design-space exploration," Design, Automation & Test in Europe Conference & Exhibition (DATE), March 2016.

Matthew M Ziegler, Hung-Yi Liu, George Gristede, Bruce Owens, Ricardo Nigaglioni, Luca P Carloni, "A Scalable Black-Box Optimization System for Auto-Tuning VLSI Synthesis Programs," Proceedings of 1st Workshop on Resource Awareness and Application Autotuning in Adaptive and Heterogeneous Computing (RES4ANT) 2016.

M Anwar, S Saha, MM Ziegler, L Reddy, "Early Scenario Pruning for Efficient Design Space Exploration in Physical Synthesis," International Conference on VLSI Design (VLSID) 2016.

R. V. Joshi, M. Ziegler, H. Wetter, C. Wandel, H. Ainspan, "14nm FinFET Based Supply Voltage Boosting Techniques for Extreme Low Vmin Operation", VLSI Circuit Symposium (VLSI), June 2015.

James Warnock, Brian Curran, John Badar, Gregory Fredeman, Donald Plass, Yuen Chan, Sean Carey, Gerard Salem, Friedrich Schroeder, Frank Malgioglio, Guenter Mayer, Christopher Berry, Michael Wood, Yiu-Hing Chan, Mark Mayo, John Isakson, Charudhathan Nagarajan, Tobias Werner, Leon Sigal, Ricardo Nigaglioni, Mark Cichanowski, Jeffrey Zitz, Matthew Ziegler, Tim Bronson, Gerald Strevig, Daniel Dreps, Ruchir Puri, Douglas Malone, Dieter Wendel, Pak-Kin Mak, Michael Blake, "22nm Next-generation IBM System z microprocessor," 2015 IEEE International Solid-State Circuits Conference (ISSCC), 2/2015.

Matthew M Ziegler, Ruchir Puri, Bob Philhower, Robert Franch, Wing Luk, Jens Leenstra, Peter Verwegen, Niels Fricke, George Gristede, Eric Fluhr, Victor Zyuban, "POWER8 design methodology innovations for improving productivity and reducing power," IEEE Proceedings of the Custom Integrated Circuits Conference (CICC), 9/2014 (**Invited**).

Ruchir Puri, Mihir Choudhury, Haifeng Qian, Matthew Ziegler, "Bridging high performance and low power in processor design," Proceedings of the 2014 international symposium on Low power electronics and design (ISLPED), 8/2014 (**Invited**).

Joshua Friedrich, Hung Le, William Starke, Jeff Stuechli, Balam Sinharoy, Eric J Fluhr, Daniel Dreps, Victor Zyuban, Gregory Still, Christopher Gonzalez, David Hogenmiller, Frank Malgioglio, Ryan Nett, Ruchir Puri, Phillip Restle, David Shan, Zeynep Toprak Deniz, Dieter Wendel, Matt Ziegler, Dave Victor, "The POWER8 TM processor: Designed for big data, analytics, and cloud environments," IEEE International Conference on IC Design & Technology, May 2014.

Eric Fluhr, Joshua Friedrich, Daniel Dreps, Victor V. Zyuban, Gregory Still, Christopher Gonzalez, Allen Hall, David Hogenmiller, Frank Malgioglio, Ryan Nett, Jose Paredes, Juergen Pille, Donald Plass, Ruchir Puri, Phillip Restle, David Shan, Kevin Stawiasz, Zeynep Toprak Deniz, Dieter Wendel, Matt Ziegler, "POWER8: A 12-core server-class processor in 22nm SOI with 7.6Tb/s off-chip bandwidth," 2014 IEEE International Solid-State Circuits Conference (ISSCC), 2/2014.

M Cho, H Xiang, H Ren, MM Ziegler, R Puri, "LatchPlanner: Latch placement algorithm for datapath-oriented high-performance VLSI designs," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2013.

MM Ziegler, GD Gristede, VV Zyuban, "Power reduction by aggressive synthesis design space exploration," IEEE International Symposium Low Power Electronics and Design (ISLPED), 8/2013

H Xiang, M Cho, H Ren, M Ziegler, R Puri, "Network flow based datapath bit slicing," ACM international symposium on Physical Design (ISPD), 2013, (**Best Paper**).

Milena Vratonjić, Matthew Ziegler, George D Gristede, Victor Zyuban, Thomas Mitchell, Ee Cho, Chandu Visweswariah, Vojin G Oklobdzija, "A new methodology for power-aware transistor sizing: free power recovery (FPR)", Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation (PATMOS), 1/2010.

MM Ziegler, VV Zyuban, GD Gristede, M Vratonjic, J Friedrich, "The opportunity cost of low power design: a case study in circuit tuning," IEEE International Symposium Low Power Electronics and Design (ISLPED), 8/2009.

Singh, R.; Ziegler, M.; Ditlow, G.; Fook-Luen Heng; Jin-Fuw Lee; Lavin, M., "Layout-aware through-process circuit analysis," International Conference on Design & Technology of Integrated Systems in Nanoscale Era DTIS, 2007, Page(s): 176-180.

Azeez Bhavnagarwala, Stephen Kosonocky, Carl Radens, Yuen Chan, Kevin Stawiasz, Uma Srinivasan, Steve Kowalczyk, Matt Ziegler, "A Sub-600mV, Fluctuation tolerant 65nm CMOS SRAM Array with Dynamic Cell Biasing," IEEE Symposium on VLSI Circuits (VLSI), 07/2007

Matthew M. Ziegler, Gary S. Ditlow, Stephen V. Kosonocky, Zhenyu (Jerry) Qi, Mircea R. Stan, "Structured and tuned array generation (STAG) for high-performance random logic," ACM Great Lakes Symposium on VLSI 2007: 257-262.

Zhenyu (Jerry) Qi, Matthew M. Ziegler, Stephen V. Kosonocky, Jan M. Rabaey, Mircea R. Stan: Multi-Dimensional Circuit and Micro-Architecture Level Optimization. ISQED 2007: 275-280.

Mircea R. Stan, Garrett Rose, Matthew Ziegler, "Hybrid CMOS/molecular Electronic Circuits," Proceedings of the International Conference on VLSI Design, Hyderabad, India, Jan. 2006.

Dan Knebel, Matthew Ziegler, Adam Butts, Stephen Kosonocky, Subhrajit Bhattacharya, Ruchir Puri, "Firefly: Qualification Vehicle for High Speed Power Gating," ACEED 2005.

M. M. Ziegler, M. R. Stan, "A Unified Design Space for Regular Parallel Prefix Adders," Design, Automation and Test in Europe (DATE), Paris, France, Feb. 2004.

M. M. Ziegler, M. R. Stan, "The CMOS/nano Interface from a Circuits Perspective," The International Symposium on Circuits and Systems (ISCAS), Bangkok, Thailand, May 2003.

M. M. Ziegler, M. R. Stan, "A Case for CMOS/nano Co-design," The International Conference on Computer-Aided Design (ICCAD), San Jose, CA, Nov. 2002.

M. M. Ziegler, G. S. Rose, M. R. Stan, "A Universal Device Model for Nanoelectronic Circuit Simulation," The IEEE Nanotechnology Conference, Washington, D. C., Aug. 2002.

M. M. Ziegler, M. R. Stan, "Design and Analysis of Crossbar Circuits for Molecular Nanoelectronics," The IEEE Nanotechnology Conference, Washington, D. C., Aug. 2002.

M. M. Ziegler, M. R. Stan, "Silicon and Molecular Electronics in terms of Information Processing Density," The Georgia Tech Conference on Nanoscience and Nanotechnology, Atlanta, GA, Sept. 2001.

M. M. Ziegler, M. R. Stan, "Flexible IP Blocks for Customized Synthesis," The International ASIC/SOC Conference, Washington, D. C., Sept. 2001.

M. M. Ziegler, A. Spanberger, G. Pai, M. Stan, K. Skadron, "Dynamic-Way Allocation for High Performance Low Power Caches," The International Conference on Parallel Architectures and Compilation Techniques (PACT 2001 – Work-in-Progress Session), Sept. 2001. Also appears in Newsletter of the IEEE Technical Committee on Computer Architecture, Oct. 2001.

M. M. Ziegler, M. R. Stan "Optimal Logarithmic Adder Structures with a Fanout of Two for Minimizing the Area-Delay Product", The International Symposium on Circuits and Systems (ISCAS), Sydney, Australia, May 2001.

## **Journal Articles (15)**

Matthew M. Ziegler, Krishnan Kailas, Xin Zhang, Rajiv V. Joshi, "Research From the IEEE IBM AI Compute and Emerging Technology Symposia," IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2019/9/2.

Sunil Shukla, Bruce Fleischer, Matthew Ziegler, Joel Silberman, Jinwook Oh, Vijayalakshmi Srinivasan, Jungwook Choi, Silvia Mueller, Ankur Agrawal, Tina Babinsky, Nianzheng Cao, Chia-Yu Chen, Pierce Chuang, Thomas Fox, George Gristede, Michael Guillorn, Howard Haynie, Michael Klaiber, Dongsoo Lee, Shih-Hsien Lo, Gary Maier, Michael Scheuermann, Swagath Venkataramani, Christos Vezyrtzis, Naigang

Wang, Fanchieh Yee, Ching Zhou, Pong-Fei Lu, Brian Curran, Leland Chang, Kailash Gopalakrishnan, "A Scalable Multi-TeraOPS Core for AI Training and Inference," IEEE Solid-State Circuits Letters, 2019/3/4.

M. M. Ziegler, R. Bertran, A. Buyuktosunoglu, P Bose, "Machine learning techniques for taming the complexity of modern hardware design," IBM Journal of Research and Development 61 (4/5), 2017.

Rajiv V. Joshi, Matthew M. Ziegler, and Holger Wetter, "A Low Voltage SRAM Using Resonant Supply Boosting," IEEE Journal of Solid-State Circuits (JSSC), Feb, 2017.

J Warnock, C Berry, MH Wood, L Sigal, Y Chan, G Mayer, M Mayo, Y-H Chan, F Malgioglio, G Strevig, C Nagarajan, S Carey, G Salem, F Schroeder, HH Smith, D Phan, RH Nigaglioni, T Strach, MM Ziegler, N Fricke, K Lind, JL Neves, SH Rangarajan, JP Surprise, JM Isakson, J Badar, D Malone, DW Plass, A Aipperspach, DF Wendel, RM Averill, R Puri, "IBM z13 circuit design and methodology," IBM Journal of Research and Development, July, 2015.

Rajiv V. Joshi, Keunwoo Kim, Rouwaida Kanj, Ajay N. Bhoj, Matthew M. Ziegler, Phil Oldiges, Pranita Kerber, Robert Wong, Terence Hook, Sudesh Saroop, Carl Radens, Chun-Chen Yeh, "Super Fast Physics-Based Methodology for Accurate Memory Yield Prediction," IEEE Transactions on Very Large Scale Integration (VLSI) Systems 03/2015.

V Zyuban, J Friedrich, DM Dreps, J Pille, DW Plass, PJ Restle, ZT Deniz, MM Ziegler, S Chu, S Islam, J Warnock, R Philhower, RM Rao, GS Still, DW Shan, E Fluhr, J Paredes, DF Wendel, CJ Gonzalez, D Hogenmiller, R Puri, SA Taylor, SD Posluszny, "IBM POWER8 circuit design and energy optimization," IBM Journal of Research and Development, 1/2015

IBM Blue Gene team, "Design of the IBM Blue Gene/Q Compute chip," IBM Journal of Research and Development," 57 (1/2), 2013.

IBM Blue Gene team, "The IBM Blue Gene Project," IBM Journal of Research and Development," 57 (1/2), 2013.

V Zyuban, J Friedrich, CJ Gonzalez, R Rao, MD Brown, MM Ziegler, H Jacobson, S Islam, S Chu, P Kartschoke, G Fiorenza, M Boersma, JA Culp, "Power optimization methodology for the ibm power7 microprocessor," IBM Journal of Research and Development, 5/2011.

Azeez J Bhavnagarwala, Stephen Kosonocky, Carl Radens, Yuen Chan, Kevin Stawiasz, Uma Srinivasan, Steven P Kowalczyk, Matthew M Ziegler, "A sub-600-mV, fluctuation tolerant 65-nm CMOS SRAM array with dynamic cell biasing," IEEE Journal of Solid-State Circuits (JSSC) , 4/2008.

G. S. Rose, M. M. Ziegler, M. R. Stan, "A Large-Signal Two-Terminal Device Model for Nanoelectronic Circuit Analysis", IEEE Transactions on VLSI Systems, vol. 12, issue 11, pp. 1201 - 1208, Nov. 2004.

M. M. Ziegler, M. R. Stan, "CMOS/nano Co-design for Crossbar-Based Molecular Electronic Systems," IEEE Transactions on Nanotechnology, vol. 2, issue 4, pp. 217-230, Dec. 2003

M. R. Stan, P. D. Franzon, S. C. Goldstein, J. C. Lach, M. M. Ziegler, "Molecular Electronics: From Devices and Interconnect to Circuits and Architecture," Proceedings of the IEEE, vol. 91, num. 11, Nov. 2003, 1940-1957.

M. M. Ziegler, C. A. Picconatto, J. C. Ellenbogen, A. DeHon, D. Wang, Z. Zhong, and C. M. Lieber, "Scalability Simulations for Nanomemory Systems Integrated on the Molecular Scale," Molecular Electronics III, Annals of the New York Academy of Sciences, vol. 1006, 2003, 312-330.

## **Book Sections (5)**

M. M. Ziegler, H.-Y. Liu, B. Owens, R. Nigaglioni, G, Gristede, J. Kwon, L. P. Carloni, "SynTunSys: A Synthesis Parameter Autotuning System for Optimizing High-Performance Processors," Machine Learning in VLSI Computer-Aided Design, Springer, Editors: Elfadel, Ibrahim (Abe) M., Boning, Duane S., Li, Xin, 2019.



MR Stan, GS Rose, MM Ziegler, "Hybrid CMOS/Molecular Integrated Circuits" in "Moore's Law: Beyond Planar Silicon CMOS and Into the Nano Era," Springer Verlag, Howard Huff editor, Springer, 2009, pp. 257-280

Mircea R. Stan, Garrett Rose, Matthew Ziegler, "A Universal Device Model for Nanoelectronic Circuit Simulation," book chapter in "EMERGING BRAIN-INSPIRED NANO-ARCHITECTURES," Springer Verlag, V. Beiu, U. Rueckert editors, 2007.

S. Das, C. A. Picconatto, G. S. Rose, M. M. Ziegler, and J. C. Ellenbogen "System-Level Design and Simulation of Nanomemories and Nanoprocessors," in Molecular and Nano Electronics Handbook, CRC Press, 5-1 - 5-39 (2007).

S. Das, G. Rose, M. M. Ziegler, C. A. Picconatto, and J. C. Ellenbogen, "Architectures and Simulations for Nanoprocessor Systems Integrated on the Molecular Scale," in Introducing Molecular Electronics, Springer-Verlag, Heidelberg (2005).

## Edited Journal & Books (2)

"From Artificial Intelligence to Brain Intelligence: AI Compute Symposium 2018 (Tutorials in Circuits and Systems)," River Publishers, 2020, ISBN-10: 8770221235.

Editors: Rajiv Joshi, Matt Ziegler, Arvind Kumar, Eduard Alarcon

<https://www.amazon.com/Artificial-Intelligence-Brain-Symposium-Tutorials/dp/8770221235>

IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) Issue 3 2019, Special Issue on "Research from the IEEE IBM AI Compute and Emerging Technology Symposia," guest editors: Matthew M. Ziegler (lead editor), Krishnan Kailas, Xin Zhang, Rajiv V. Joshi.

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## INVITED EXTERNAL TALKS

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9/2019 – "Design Challenges at Scale for Emerging AI Devices and Architectures," The Future of Artificial Intelligence Hardware Systems: A Forum organized by Mubadala, SRC, and Khalifa University.

8/2018 – "Deep Learning Acceleration: Opportunities Across the Stack," Cross-layer Computing Summer School: Circuits to System, Northwestern University.

12/2015 – "Industrial Strength VLSI Design Automation by Merging Human and Computer Skills," University of Virginia.

9/2014 – "POWER8 design methodology innovations for improving productivity and reducing power," IEEE Proceedings of the Custom Integrated Circuits Conference (CICC).

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## BIOGRAPHY

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**Dr. Matthew M. Ziegler** is a Principal Research Staff Member at the IBM T. J. Watson Research Center, Yorktown Heights, NY. He received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, in 2004. Since joining IBM Research in 2004, he received several technical accomplishment awards in the areas of processor design, design automation, and low power design. Dr. Ziegler has directly participated in the design of IBM's Power Systems, z Systems, and BlueGene families of products. His research has recently focused on AI accelerator design, machine learning for CAD, VLSI design productivity, optimization, and low power design. This work has led to design methodologies and design automation systems used throughout IBM processor designs. He is a recipient of the 2018 Mehboob Khan Award from the Semiconductor Research Corporation and is a member of the IBM Academy of Technology. He has served on various conference committees, including being an ISLPED 2018 TPC chair and an ISLPED 2019 general chair. He has also been a TPC chair for the 2017 IEEE IBM Emerging Technology Symposium and the 2018-2020 IEEE IBM AI Compute Symposia.