- **Mark J. Cianchetti**
  - **Title:** Inter and Intra Die Photonic Communication for Future Chip Multiprocessors
  - **Abstract:** Tens and eventually hundreds of processing cores are projected to be integrated onto future microprocessors, making the global interconnect a key component to achieving scalable chip performance within a given power envelope. CMOS-compatible nanophotonics has emerged as a leading candidate for replacing global wires beyond the 22 nm timeframe. In this talk I will present a hybrid electrical/optical router for future large scale, cache coherent multicore microprocessors. The heart of the router is a low-latency optical crossbar that uses simple predecoded source routing and switch state prediction to transmit cache-line sized packets several hops in a single clock cycle under contentionless conditions. When contention exists, the router makes use of electrical buffers to store blocked packets. Overall, our optical router achieves better network performance than a state-of-the-art electrical baseline in a mesh topology while consuming less network power.
  - **Bio:** Mark Cianchetti is a fifth year Ph.D. student working in the Computer Systems Laboratory at Cornell University under the supervision of Professor David Albonesi. His research focuses on the design of optical interconnection networks in future chip multiprocessors. He received two B.S. degrees from the University of Buffalo in 2006 and is a recent recipient of an Intel Fellowship. In his free time Mark enjoys oil painting, exercising and playing the piano.