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A High-Performance Sorting Algorithm for Multicore Single-Instruction Multiple-Data Processors

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Abstract

Many sorting algorithms have been studied in the past, but there are only a few algorithms that can effectively exploit both SIMD instructions and thread-level parallelism. In this paper, we propose a new high-performance sorting algorithm, called Aligned-Access sort (AA-sort), for exploiting both the SIMD instructions and thread-level parallelism available on today's multicore processors. Our algorithm consists of two phases, an in-core sorting phase and an out-of-core merging phase. The in-core sorting phase uses our new sorting algorithm that extends combsort to exploit SIMD instructions. The out-of-core algorithm is based on mergesort with our novel vectorized merging algorithm. Both phases can take advantage of SIMD instructions. The key to high performance is eliminating unaligned memory accesses that would reduce the effectiveness of SIMD instructions in both phases. We implemented and evaluated the AA-sort on PowerPC 970MP and Cell Broadband Engine platforms. In summary, a sequential version of the AA-sort using SIMD instructions outperformed IBM's optimized sequential sorting library by 1.8 times and bitonic merge sort using SIMD instructions by 3.3 times on PowerPC 970MP when sorting 32 million random 32-bit integers. Also, a parallel version of AA-sort demonstrated better scalability with increasing numbers of cores than a parallel version of bitonic merge sort on both platforms.

Keywords: Sorting, Merging, SIMD, VMX, Parallel Algorithms.

1. INTRODUCTION

Many modern high-performance processors provide multiple hardware threads within one physical processor with multiple cores and simultaneous multithreading. Many processors also provide Single Instruction Multiple Data (SIMD) instructions, such as the SSE instruction set of the x86 or the VMX instruction set of the PowerPC. They can operate on multiple data values in parallel to accelerate computationally intensive programs for a broad range of applications.

An obvious advantage of the SIMD instructions is the degree of data parallelism available in one instruction. In addition, they allow programmers to reduce the number of conditional branches in their programs. For example, a program can select the smaller or larger value from each element's pair of two vectors without conditional branches. Branches can potentially incur pipeline stalls and thus limit the performance of superscalar processors with long pipeline stages. Therefore, the benefit of reduction in the number of conditional branches is significant for many workloads. For example, Zhou and Ross [1] reported that SIMD instructions can accelerate many database operations, such as scan operations and join operations, by removing branch overhead.

Sorting is one of the most important building blocks for operating systems and many commercial and scientific applications, such as data-base management systems [2]. Hence many sequential and

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parallel sorting algorithms have been studied in the past [3, 4]. However popular sorting algorithms, such as quicksort, are not able to exploit SIMD instructions efficiently. For example, a VMX instruction or a SSE instruction can load or store 128 bits of data between a vector register and memory with one instruction, but this is effective only when the data is aligned on a 128-bit boundary. Many sorting algorithms require unaligned or element-wise memory accesses, which incur additional overhead and attenuate the benefits of SIMD instructions. There is no known technique to remove unaligned memory accesses from quicksort.

In this paper[†], we propose a new high-performance sorting algorithm suitable for exploiting both the SIMD instructions and thread-level parallelism available on today's multicore processors. We call the new algorithm Aligned-Access sort (AA-sort). The AA-sort consists of two phases: an in-core sorting phase and an out-of-core merging phase. Both phases can take advantage of the SIMD instructions and can also run in parallel with multiple threads.

The in-core sorting phase uses our new algorithm that extends combsort [5] for exploiting SIMD instructions. This makes it possible to eliminate all unaligned memory accesses and fully exploit the SIMD instructions. The key idea to improve combsort is to first sort the input data into a transposed order using vector comparisons, and then reorder it into the desired order. The computational complexity for both the combsort and our vectorized combsort is $O(N \bullet \log(N))$[‡] on average, and $O(N^2)$ in the worst case when sorting N elements. In our AA-sort, we avoid the worst case computational time of the vectorized combsort by switching from the vectorized combsort to our vectorized mergesort, whose complexity is $O(N \bullet \log(N))$ even for the worst case, when the number of iterations exceeds a constant threshold. Thus the complexity of $O(N \bullet \log(N))$ is guaranteed for the in-core sorting of the AA-sort. Disadvantages of the vectorized combsort include poor memory access locality, so we combine it with another sorting algorithm in the out-of-core merging phase to make it possible for the entire AA-sort to use the cache more efficiently.

The out-of-core merging phase is based on mergesort and employs our new vectorized merge algorithm. It has better memory access locality than our in-core algorithm. Its computational complexity is $O(N \bullet \log(N))$ even in the worst case.

The complete AA-sort algorithm first divides all of the data into blocks that fit in the L2 cache of each processor core. Next it sorts each block in the in-core sorting phase. Finally it merges the sorted blocks with our vectorized merge algorithm to complete the sorting in the out-of-core merging phase. Both phases can be executed by multiple threads in parallel. The entire AA-sort has the computational complexity of $O(N \bullet \log(N))$. Also it can be executed in parallel by multiple threads with the complexity of $O(N \bullet \log(N)/k)$ assuming the number of threads, k, is smaller than the number of blocks for the in-core phase.

We implemented and evaluated the AA-sort on a system with 4 cores of the PowerPC 970MP

[†] A preliminary version of this paper was published in proceedings of the Sixteenth IEEE Parallel Architecture and Compilation Techniques (PACT 2007) [6]. This paper adds more descriptions of our new algorithm. It also includes more detailed analysis of the results of our measurements, including the effects of important parameters on performance.

[‡] log refers to logarithm with base 2 unless a different value is specified.

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processor and a system with 16 cores of the Cell Broadband Engine (Cell BE) processor [7]. In summary, a sequential version of the AA-sort using SIMD instructions outperformed IBM's optimized sequential sorting library by 1.8 times and the bitonic merge sort that uses SIMD instructions, the best existing sorting algorithm for SIMD processors, by 3.3 times on the PowerPC 970MP when sorting 32 million random 32-bit integers. The performance of the AA-sort did not depend on key distributions of the input data by eliminating the data-dependent conditional branches. Also, a parallel version of the AA-sort demonstrated better scalability with increasing numbers of cores than a parallel version of the bitonic merge sort. It achieved a speed up of 12.2 for 16 cores on the Cell BE, while the bitonic merge sort achieved a speedup of 7.1. As a result, the AA-sort was 4.2 times faster on 4 cores of the PowerPC 970MP and 4.9 times faster on 16 cores of the Cell BE processor than the bitonic merge sort when sorting 32 million random 32-bit integers.

The main contribution of this paper is a new high-performance sorting algorithm that can effectively exploit SIMD instructions. It consists of two algorithms: a vectorized combsort and a vectorized mergesort. In our vectorized combsort, it is possible to eliminate all unaligned memory accesses from combsort. For the vectorized mergesort, we proposed a novel linear-time merge algorithm that can take advantage of the SIMD instructions. We show that our AA-sort achieves higher performance and scalability with increasing numbers of processor cores than the best known algorithms.

The rest of the paper is organized as follows. Section 2 gives an overview of the SIMD instructions we use for sorting. Section 3 discusses related work. Section 4 de-scribes the AA-sort algorithm. Section 5 discusses our experimental environment and gives a summary of our results. Finally, Section 6 draws conclusions.

2. SIMD INSTRUCTION SET

In this paper we use the Vector Multimedia eXtension [8] (VMX, also known as AltiVec) instructions of the PowerPC instruction set to present our new sorting algorithm. It provides a set of 128-bit vector registers, each of which can be used as sixteen 8-bit values, eight 16-bit values, or four 32-bit values. The following VMX instructions are useful for sorting: vector compare, vector select, and vector permutation.

The vector compare instruction reads from two input registers and writes to one output register. It compares each value in the first input register to the corresponding value in the second input register and returns the result of comparisons as a mask in the output register.

The vector select instruction takes three registers as the inputs and one for the output. It selects a value for each bit from the first or second input registers by using the contents of the third input register as a mask for the selection.

The vector permutation instruction also takes three registers as the inputs and one for the output. The instruction can reorder the single-byte values of the input arbitrarily. The first two registers are treated as an array of 32 single-byte values, and the third register is used as an array of indexes to pick 16 arbitrary bytes from the input register.

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These instructions are not unique to the VMX instruction set and thus our algorithm can be implemented using other SIMD instruction sets, such as the SPE instruction set of Cell BE and the SSE4 instruction set of the x86. We show our implementation of our algorithm on Cell BE in this paper and Chhugani *et al.* [9] described an implementation of a part of our algorithm using the SSE4 [10].

3. RELATED WORK

Many sorting algorithms have been proposed in the past. Quicksort is one of the fastest algorithms used in practice, and hence there are many optimized implementations of quicksort available. However there is no known technique to implement quicksort using existing SIMD instructions.

Radixsort is another sorting algorithm widely used today. It has a smaller computational complexity than any comparison-based algorithms such as quicksort or our AA-sort. However its scattered memory accesses make it difficult for radixsort to exploit SIMD instructions. The scattered memory accesses also tend to increase the required main memory bandwidth and thus the radixsort may suffer from a poor scalability on multicore processors because the memory bandwidth tends to become a bottleneck in systems with multicore processors [11].

Sanders and Winkel [12] pointed out that the performance of sorting on today's processors is often dominated by pipeline stalls caused by branch mispredictions. They proposed a new sorting algorithm, named super-scalar sample sort (sss-sort), to avoid such pipeline stalls by eliminating conditional branches. They implemented the sss-sort by using the predicated instructions of the processor and showed that the sss-sort achieves up to 2 times higher performance over the STL sorting function delivered with gcc. Our algorithm can also avoid pipeline stalls caused by branch miss predictions. Moreover, our algorithm makes it possible to take advantage of the data parallelism of SIMD instructions.

There are some sorting algorithms suitable for exploiting SIMD instructions [13, 14, 15]. They were originally proposed in the context of sorting on graphics processing units (GPUs), which were powerful programmable processors with SIMD instruction sets.

Govindaraju *et al.* [15] presented a sorting algorithm called GPUTeraSort that improved on bitonic merge sort [16]. The bitonic merge sort has computational complexity of $O(N \bullet (\log(N))^2)$ and it can be executed by up to N processors in parallel. The GPUTeraSort improves this algorithm by altering the order of comparisons to improve the effectiveness of the SIMD comparisons and also by increasing the memory access locality. Comparing the AA-sort to the GPUTeraSort, both algorithms can be effectively implemented with SIMD instructions and both can exploit thread-level parallelism. An advantage of our AA-sort is the computational complexity of $O(N \bullet \log(N))$, which is the optimal complexity for any comparison-based sorting algorithm, while the complexity for the GPUTeraSort (or other bitonic merge sort variants) is $O(N \bullet (\log(N))^2)$.

Gedik *et al*. [17] presented a sorting algorithm for Cell BE called the CellSort. They also used the bitonic merge sort as their computing kernel to exploit the SIMD instruction set and thread-level parallelism of the processor. Thus the computational complexity of their algorithm was larger than

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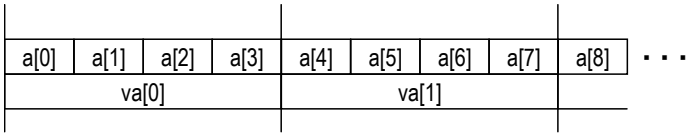

Fig. 1. Data structure of the array to be sorted.

ours.

Furtak *et al*. [18] showed the benefits of exploiting SIMD instructions for sorting very small arrays. They demonstrated that replacing only the last few steps of quicksort by a sorting network implemented with SIMD instructions improved the performance of the entire sort by up to 22%. They evaluated the performance benefits for the SSE instructions and the VMX instructions. The AA-sort can take advantage of SIMD instructions not only in the last part of the sorting, but also for entire stages.

Cederman and Tsigas [19] demonstrated that their quicksort implementation on recent NVIDIA GPUs achieved much better performance than quicksort on general-purpose CPUs or the GPUTeraSort running on the same GPUs. Their quicksort for GPUs exploits the flexible memory access mechanisms of the recent GPUs. With these GPUs, each slot of a vector load or store instruction can access an arbitrary memory address, while the corresponding VMX or SSE instructions can only access properly-aligned contiguous 128-bit blocks of data. Using this flexible memory access, each slot of the GPU's vector instructions can act as a separate thread. NVIDIA calls this processor architecture SIMT (single-instruction, multiple-thread) in contrast to the traditional SIMD [20]. Our AA-sort targets the SIMD processors, which have more limitations than the SIMT processors.

4. AA-SORT ALGORITHM

In this section, we present our new sorting algorithm called AA-sort. We use 32-bit integers as the data type of the elements to be sorted. Hence one 128-bit vector register contains four values. Note that our algorithm is not limited to this data type and degree of data parallelism as long as the SIMD instructions support them. We assume the first element of the array to be sorted is aligned on a 128-bit boundary and the number of elements in the array, N, is a multiple of the degree of data parallelism of the SIMD instructions for ease of explanation. Fig. 1 illustrates the layout of the array, $a[N]$. The array of integer values $a[N]$ is equivalent to an array of vector integers $va[N/4]$. A vector integer element $va[i]$ consists of the four integer values of $a[i*4]$ to $a[i*4+3]$.

AA-sort consists of two algorithms, a vectorized combsort sort and a vectorized merge sort. The overall AA-sort executes the following phases using the two algorithms:

1. Divide all of the data into blocks that fit into the cache of the processor and sort each block with the vectorized combsort (in-core sorting phase).
2. Merge the sorted blocks with the vectorized mergesort (out-of-core merging phase).

First we present these two vectorized sorting algorithms and then illustrate the overall sorting scheme.

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```
gap = N / SHRINK_FACTOR;
while (gap > 1) {
   for (i = 0; i < N - gap; i++)
      if (a[i] > a[i+gap]) swap(a[i], a[i+gap]);
   gap /= SHRINK_FACTOR;
}
do {
   for (i = 0; i < N - 1; i++)
      if (a[i] > a[i+1]) swap(a[i], a[i+1]);
} while( not fully sorted );
```

Fig. 2. Pseudocode of combsort.

4.1 Vectorized Combsort

Our vectorized combsort improves on combsort [5], an extension to bubble sort. Bubble sort compares each element to the next element and swaps them if they are out of sorted order. Combsort compares and swaps two non-adjacent elements. Comparing two values with large separations improves the performance drastically, because each value moves toward its final position more quickly. Fig. 2 shows the pseudocode of combsort. The separation (labeled *gap* in Fig. 2) is divided by a number, the *shrink factor*, in each iteration until it becomes one. The authors used 1.3 for the shrink factor. Then the final loop is repeated until all of the data is sorted. The computational complexity of combsort is O(N•log(N)) on average.

The fundamental operation of many sorting algorithms including combsort and bitonic merge sort is to compare two values and swap them if they are out of order. Each conditional branch in this operation will be taken in arbitrary order with roughly 50% probability for random input data, and therefore it is very hard for branch prediction hardware to predict the branches. This operation can be implemented using vector compare and vector select instructions without conditional branches.

Combsort has two problems that reduce the effectiveness of SIMD instructions: 1) unaligned memory accesses and 2) loop-carried dependencies. Regarding the unaligned memory accesses, combsort requires unaligned memory accesses when the value of the gap is not a multiple of the degree of data parallelism of the SIMD instructions. A loop-carried dependency prevents exploitation of the data parallelism of the SIMD instructions when the value of the gap is smaller than the degree of data parallelism.

In our vectorized combsort, we resolved these problems with combsort. The key idea of our improvement is to first sort the values into the *transposed* order and reorder the sorted values into the original order after the sorting. Fig. 3 shows the steps of our vectorization technique for combsort. It consists of the following 3 steps:

1. sort values within each vector,
2. execute combsort to sort the values into the transposed order, and then
3. reorder the values from the transposed order into the original order.

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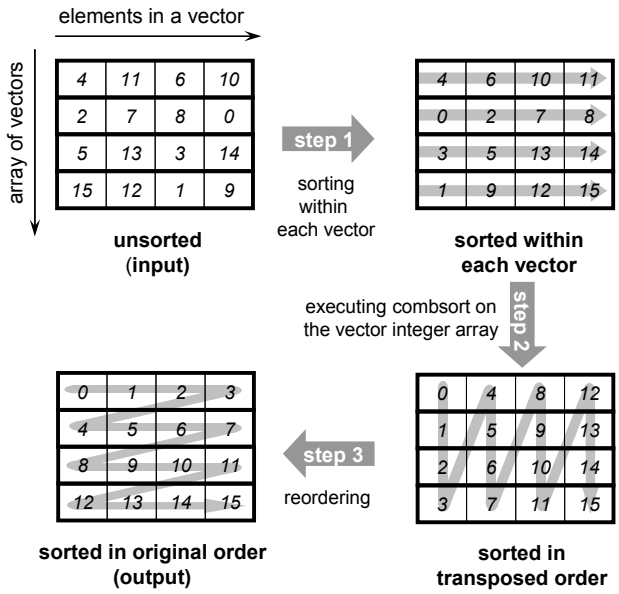

Fig. 3. Steps of our vectorized combsort algorithm for sorting 16 values (4 vectors).

Fig. 3 shows an example for an array with 16 integers (or four vector integers).

Step 1 sorts four values in each vector integer $va[i]$ ($0 \le i < N/4$, here N=16 in Fig 3). This step corresponds to the loops with the gaps of $N/4$, $N/4*2$, and $N/4*3$ in combsort, because the gap between consecutive elements in one vector register is $N/4$ in the transposed order. The sorting for values in a vector register can be implemented as a sorting network using vector comparison and vector permutation instructions [18].

Step 2 executes combsort on the vector integer array $va[N/4]$ in the transposed order. Fig. 4 shows pseudocode for our vectorized combsort algorithm. In this code, *vector_cmpswap* is an operation that compares and swaps values in each element of the vector register A with the corresponding element of the vector register B as shown in Fig. 5. This operation can be implemented using a pair of vector minimum and maximum instructions or one vector compare instruction and two vector select instructions. Similarly *vector_cmpswap_skew* is an operation that compares and swaps the first to third elements of the vector register A with the second to fourth elements of the vector register B. It does not change the last element of the vector register A and the first element of the vector register B. Both operations can be implemented using SIMD instructions. Comparing the code of Fig. 4 to the code of the original combsort in Fig. 2, the innermost loop is divided into two loops with these two operations. With these two loops, all of the values are compared and swapped with the values for the distance of the *gap* in the transposed order. The original loop was divided into two because the pairs to be compared may reside in the same positions of the vector registers or in different positions.

The last do-while loop of step 2 executes bubble sort to assure the correct order of the output. In order to guarantee against the worst case performance of $O(N^2)$ caused by the bubble sort, we cancel the last loop in the Step 2 after executing a constant number of iterations. In our AA-sort that uses the vectorized combsort in the in-core phase, we use 10 for the threshold and switch to the

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```
/* Step 1 */
for (i = 0; i < N/4; i++)
   sort_within_a_vector(va[i]);

/* Step 2 */
gap = (N/4) / SHRINK_FACTOR;

while (gap > 1) {
   /* straight comparisons          */
   for (i = 0; i < N/4 - gap; i++)
         vector_cmpswap(va[i], va[i+gap]);

   /* skewed comparisons when i+gap exceeds N/4      */
   for (i = N/4 - gap; i < N/4; i++)
         vector_cmpswap_skew(va[i], va[i+gap – N/4]);

   /* dividing gap by the shrink factor */
   gap /= SHRINK_FACTOR;
}

loop_count = 0;
do {     /* executing bubble sort */
   for (i = 0; i < N/4 - 1; i++)
         vector_cmpswap(va[i], va[i+1]);
   vector_cmpswap_skew(va[N/4-1], va[0]);
} while( not totally sorted && loop_count++ < THRESHOLD);

/* abort and switch another algorithm when loop_count reaches threshold */
if (not totally sorted) return false;

/* Step 3 */
for (i = 0; i < N/16; i++)
   transpose_4x4_block(va[i*4], va[i*4+1], va[i*4+2], va[i*4+3]);

for (i = 0; i < N/4; i++)
   move_vector_to_desired_location(va[i]);

return true; /* completed successfully */
```

Fig. 4. Pseudocode of our vectorized combsort.

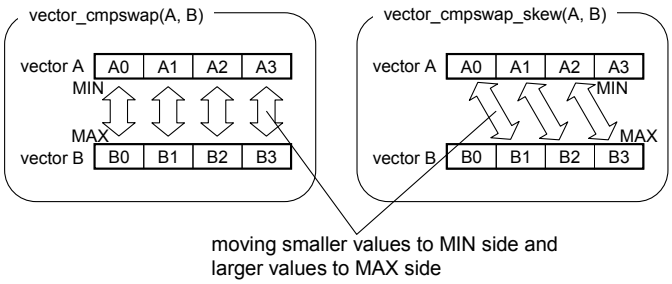

Fig. 5. The vector_cmpswap and vector_cmpswap_skew operations.

vectorized mergesort, whose complexity is O(N•log(N)) even for the worst case, when the execution of the combsort is canceled. In practice, however, we have never observed the cancellations of the vectorized combsort in our evaluations.

Step 3 reorders the sorted values into the correct order. This step does not require data-dependent conditional branches because it only moves each element in predefined orders, and hence the

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reordering does not incur troublesome overhead. Vector permutation instructions can efficiently execute this step when the number of vectors is a multiple of the number of elements in each vector, four in this example. For example, the four vectors in Fig. 3 can be reordered by using only 8 vector permutation instructions. The first four permutations swap the upper-right 2x2 block (consists of 8, 9, 12, and 13) and the lower-left one (2, 3, 6, and 7). The next four permutations swap the upper-right value and lower-left value in each 2x2 block (such as 1 and 4). After applying this vectorized transposition technique, all of the vectors contains four sequential values, and thus the program can reorder the values into the original order by simply moving vectors with vector load and vector store instructions. For the final data moves, our implementation uses a temporary memory space with the same size as the data. This step also does not cause any unaligned memory accesses.

In summary, our vectorized combsort consists of three steps. All three of the steps can be executed by SIMD instructions without unaligned memory accesses. Also, all of them can be implemented with a negligible number of data-dependent conditional branches.

Let N be the total number of elements to be sorted. The computational complexity of Step1 and Step3 is $O(N)$, and that of Step 2 is the same as that of combsort, $O(N \bullet \log(N))$ on average. Thus the computational complexity of the entire algorithm is dominated by Step 2. In Step2, we cancel the execution of the vectorized combsort if the number of iterations exceeds a constant threshold and switch to the vectorized merge sort to guarantee the $O(N \bullet \log(N))$ complexity even for the worst case.

Our vectorized combsort suffers from poor memory access locality. Thus its performance may degrade if the data cannot fit into the cache of the processor. We propose another sorting algorithm, the vectorized mergesort, which takes that problem into account.

4.2 Vectorized Mergesort

For the vectorized mergesort, we propose an innovative method to integrate the odd-even merge algorithm [16] implemented with SIMD instructions into a traditional merge algorithm. Our method makes it possible for the merge operations to take advantage of SIMD instructions while still retaining the computational complexity of $O(N)$. The odd-even merge and the bitonic merge, also suitable for implementing with SIMD instructions, have the computational complexity of $O(N \bullet \log(N))$ instead of the complexity of $O(N)$ of our algorithm.

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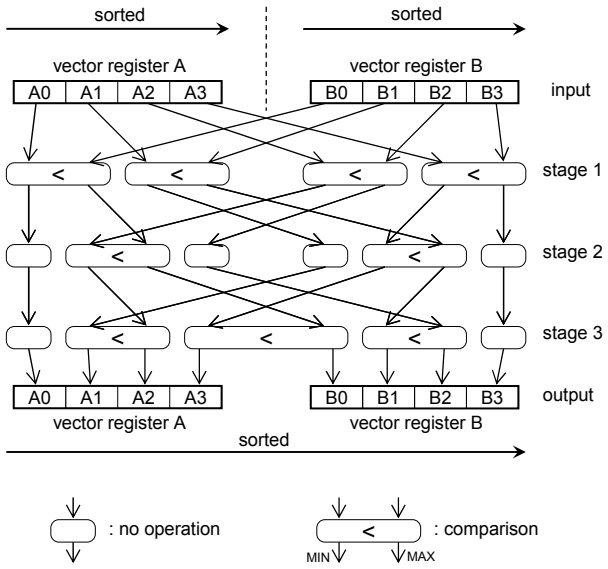

Fig. 6. Data flow of odd-even merge operation for two vector registers.

Fig. 6 shows the data flow of the odd-even merge operation for eight values stored in the two vector registers, which contain four sorted values each. In the figure the boxes with inequality symbols signify comparison operations. Each of them reads two values from the two inputs (one each) and sends the smaller value to the left output and the larger one to the right. The odd-even merge operation requires $\log(P)+1$ stages to merge two vector registers, each of which contain P elements. Here $P=4$ and $\log(P)+1=3$. Each stage executes only one vector compare, two vector select, and one or two vector permutation instructions. If an SIMD instruction set does not support a vector permutation operation, then repeating a vector_cmpswap operation and a rotation of one vector register can substitute for the odd-even merge. However this requires P stages instead of $\log(P)+1$ stages.

The merge operation for two large arrays stored in memory can be implemented using this merge operation for the vector registers. Fig. 7 shows the pseudocode for merging of two vector integer arrays *va* and *vb*. In this code, the *vector_merge* operation is the merge operation for the vector registers shown in Fig. 6. In each iteration, this code

1. executes a merge operation of two vector registers, *vMin* and *vMax*,
2. stores the contents of *vMin*, the four smallest values, as output,
3. compares the next element of each input array, and
4. loads four values into *vMin* from the array whose next element is smallest and advances the pointer for the array.

Loading new elements from only one input array is sufficient, because at least one of the next elements of each input array must be larger than all of the data values in *vMax* and hence the larger of the two next elements must not be contained in the next four output values. There is only one conditional branch for the output of every P elements, while the naive merge operation requires one conditional branch for each output element.

The vectorized mergesort recursively repeats the merge operation described earlier. It does not

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```
aPos = bPos = outPos = 0;
vMin = va[aPos++];
vMax = vb[bPos++];

while (aPos < aEnd && bPos < bEnd) {

   /*    merge vMin and vMax */
   vector_merge(vMin, vMax);

   /*    store the smaller vector as output*/
   vMergedArray[outPos++] = vMin;

   /*    load next vector and advance pointer          */
   /*    a[aPos*4] is first element of va[aPos]        */
   /*    and b[bPos*4] is that of vb[bPos]             */
   if (a[aPos*4] < b[bPos*4])
         vMin = va[aPos++];
   else
         vMin = vb[bPos++];
}
```

Fig. 7. Pseudocode of the merge operation in memory.

require any unaligned memory accesses. However, it has lower performance than our vectorized combsort for the small amounts of data that can fit in the cache because the vectorized mergesort reduces the number of data-dependent conditional branches but still uses them while the vectorized combsort totally eliminates them. In contrast, the vectorized merge sort achieves higher performance than the vectorized combsort when the data cannot fit in the cache. This is because the vectorized mergesort has much better memory access locality compared to the vectorized combsort.

In order to reduce the required memory bandwidth, which limits the performance of sorting when using many cores, we use a multi-way merge technique [4] with the out-of-core phase in our experimental implementation of the AA-sort. We employ a 4-way merge, so input data is read from 4 streams and output into one merged output stream. This does not change the required number of comparisons but reduces the number of merging stages from $\log_2(N/B)$ to $\log_4(N/B)$. The vectorized mergesort scans all of the elements in merging stage and thus reducing the number of stages also reduces the required memory bandwidth by improving memory access locality. To execute the 4-way merge using SIMD instructions, we generate two temporary arrays each having 1 K elements. At the beginning of the merging operation, we fill the first temporary array by merging the first two input streams and the second temporary array by merging other two input streams with the vectorized merge operations. Then the output stream is generated by merging those two temporary arrays. When a temporary array becomes empty while generating the final output stream, we refill the temporary array by going back to the merging of two input arrays for the temporary array. We repeat these operations until we hit the ends of all input streams.

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```
/* in-core sorting phase */
numBlocks = N / B;
blockSize = B;
blocksPerThread = numBlocks / numThreads;
for (i = blocksPerThread * myThreadID; i < blocksPerThread * (myThreadID+1); i++) {
   /* parameters are a pointer to the input data, a number of elements to sort,
         and a threshold to cancel executing combsort */
   sorted = vectorized_combsort(data[blockSize*i], blockSize, 10);

   /* switch to vectorized mergesort if combsort did not completed within the predifined number of iterations */
   if (!sorted) vectorized_mergesort(data[blockSize*i], blockSize);
}

/* out-of-core merging phase */
while (numBlocks > 1) {
   blocksPerThread = numBlocks / numThreads;
   /* if there are enough blocks to execute 4-way merge by each thread */
   if (numBlocks >= numThreads * 4) {
      for (i = blocksPerThread * myThreadID; i < blocksPerThread * (myThreadID+1); i+=4)
         /* parameters are four pointers to the input data buffers, a pointer for the output buffer, */
         /* and a number of elements to merge in each input data */
         vectorized_4way_merge(data[blockSize*i   ], data[blockSize*i+1],
                               data[blockSize*i+2], data[blockSize*i+3],
                               tmp [blockSize*i   ], blockSize);
      numBlocks /= 4;   blockSize *= 4;
   }
   /* if there are enough blocks to execute 2-way merge by each thread */
   else if (numBlocks >= numThreads * 2) {
      for (i = blocksPerThread * myThreadID; i < blocksPerThread * (myThreadID+1); i+=2)
         vectorized_2way_merge(data[blockSize*i], data[blockSize*i+1],
                               tmp [blockSize*i], blockSize);
      numBlocks /= 2;   blockSize *= 2;
   }
   /* if there are not enough blocks to work all thread independently */
   else {
      barrier(); /* a barrier synchronization among threads required before cooperative merge operations */
      numThreadsToCooperate = numThreads / (numBlocks / 2);
      assignedBlock = myThreadID / numThreadToCooperate;
      vectorized_merge_with_multiple_threads(data[ 2*assignedBlock       * blockSize],
                                             data[(2*assignedBlock+1) * blockSize],
                                             tmp [ 2*assignedBlock       * blockSize], blockSize,
                                             blockSize, numThreadsToCooperate, myThreadID);
      numBlocks /= 2;   blockSize *= 2;
   }
   swap(data, tmp);   numMergeStages++;   /* swap pointers for the input and output buffers */
}
if (numMergeStages & 1) { memcpy(tmp, data, N * sizeof(element type)); }
```

Fig. 8. Pseudocode of the entire AA-sort algorithm

4.3 Overall Parallel Sorting Scheme of AA-Sort

The overall AA-sort executes the following phases using the two algorithms:

1. Divide all of the data to be sorted into blocks that fit in the cache or the local memory of the processor and sort each block with the vectorized combsort in parallel using multiple threads, where each thread processes an independent block. (in-core sorting phase)
2. Merge the sorted blocks with the vectorized mergesort using multiple threads. (out-of-core merging phase)

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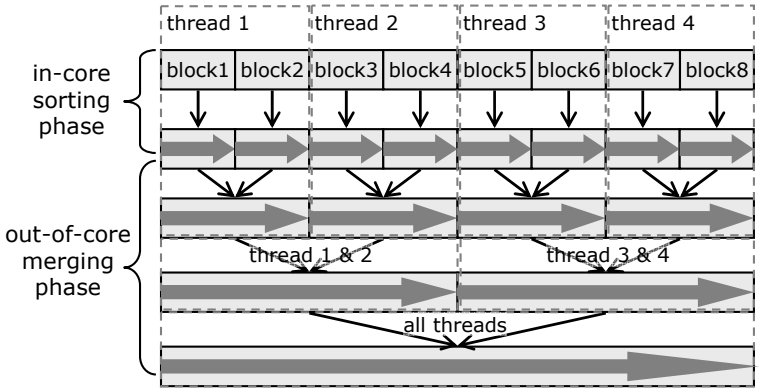

Fig. 9. An example of the entire AA-sort process, where number of blocks (N/B) = 8 and the number of threads (k) = 4.

Fig. 8 shows the pseudocode for the entire AA-sort scheme and the Fig. 9 depicts an example of the entire AA-sort execution with four parallel threads.

The block size for the in-core sorting phase is an important parameter. The selection of the block size depends on bandwidth and latency for each level of memory hierarchy of the target system. On the PowerPC 970MP processors, for example, half of the size of L2 cache was best for the block size because its L2 cache was fast enough to keep the processor core busy even though there were many L1 cache misses. We discuss how we chose the block size in Section 5.2.

If the total number of elements of data to sort is N and the number of elements in one block is B, then the number of blocks for the in-core algorithm is (N/B). The computational complexity of the in-core sorting of each block is $O(B \bullet \log(B))$. We avoid the worst case computational time of $O(B^2)$ and guarantee the complexity for the in-core sorting by switching from the vectorized combsort to vectorized mergesort. Hence the total computational complexity of the in-core sorting phase is $(N/B) \bullet O(B \bullet \log(B)) = O(N \bullet \log(B))$. The sorting of each block is independent of the other blocks, so they can run in parallel on multiple threads up to the number of blocks. Thus the total complexity of the in-core phase with multiple threads is $O(N \bullet \log(B)/k)$ assuming the number of threads, k, is smaller than the number of blocks, (N/B).

In the out-of-core merging phase, merging the sorted blocks involves $\log(N/B)$ stages and the computational complexity of each stage is $O(N)$, and thus the total computational complexity of this phase is $O(N \bullet \log(N/B))$, even in the worst case. Note that this complexity is not changed with the 4-way merge technique. With the 4-way merge, the number of stages is reduced from $\log_2(N/B)$ to $\log_4(N/B) = 1/2 \bullet \log_2(N/B)$, but the number of comparisons involved in one stage doubles. It only reduced the required system memory bandwidth. The total complexity of the out-of-core merging phase with k threads is $O(N \bullet \log(N/B)/k)$. For parallelizing the last $\log(k)$ stages of the out-of-core phase, the number of blocks becomes smaller than the number of threads, and hence multiple threads must cooperate on one merge operation to fully exploit the thread-level parallelism [21].

The entire AA-sort has the computational complexity of $O(N \bullet \log(N))$, where $O(N \bullet \log(B))$ for the in-core phase and $O(N \bullet \log(N/B))$ for the out-of-core phase, even for the worst case. Also it can be executed in parallel by multiple threads with complexity of $O(N \bullet \log(N)/k)$ assuming the number of threads is smaller than the number of blocks, (N/B).

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Table 1. Comparisons of Algorithms

algorithm	SIMD	thread parallel	complexity	
			average	worst
AA-sort	Yes	Yes	N•log(N)	←
bitonic merge sort	Yes	Yes	N•(log(N))^2	←
ESSL	No	No	N•log(N)	N^2
STL (introsort)	No	No	N•log(N)	←

N: number of data items to sort

4.4 Sorting of {Key, Data} Pairs

In real-world workloads, sorting is mostly used to reorder data structures according to their keys. We can extend the AA-sort for such purposes. To that end, we consider sorting for pairs consisting of a key of a 32-bit integer value and a 32-bit piece of associated data, such as a pointer to the data structure that contains the key. Assuming the keys and the attached data are stored in distinct arrays, the comparing and swapping operations can be implemented by using the results of the comparisons for the key to move both the keys and the data. When the keys and attached data are stored in an array one after another, comparing and swapping of {key, data} pairs can be implemented by adding one vector permutation instruction after the vector compare instruction to replace the result of the comparison of the data with the result of the comparison of the keys. Hence the data always move with the associated keys in both cases.

5. EXPERIMENTAL RESULTS

We implemented the AA-sort and the bitonic merge sort for the PowerPC 970MP [22] and the Cell BE [7] with and without using the SIMD instructions. We implemented the bitonic merge sort by following the GPUTeraSort [15] for comparison because it is one of the best existing sorting algorithms for SIMD instructions. The CellSort by Gedik [17] uses the almost same algorithm for its sorting kernel. Our measured sorting times for the bitonic merge sort on the Cell BE were quite comparable to the results of the CellSort on the Cell BE shown in their paper. For example, Gedik's paper reported that sorting 32 M random integers using 16 SPE cores took 0.746 seconds for the CellSort (on 3.2-GHz Cell BE), while this took 0.776 seconds with our implementation of the bitonic merge sort (on 2.4-GHz Cell BE).

We also evaluated two library functions, IBM's Engineering and Scientific Subroutine Library (ESSL) version 4.2 and the STL library delivered with gcc that implements the quicksort variant called introsort [23], on the PowerPC 970MP. Table 1 summarizes the characteristics of each algorithm.

The PowerPC 970MP system used for our evaluation was equipped with two 2.5 GHz dual-core PowerPC 970MP processors and 8 GB of system memory. In total, the system had 4 cores, each of which had 1 MB of L2 cache memory. Linux kernel 2.6.20 was running on the system. We also evaluated the performance of the sorting programs on a system equipped with two 2.4 GHz Cell BE processors with 1 GB of system memory. The Cell BE is an asymmetric multicore processor that

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combines a PowerPC core with eight accelerator cores called SPEs. We used only the SPE cores for sorting. Thus, 16 SPE cores with 256 KB local memory each were available on the system. This system ran Linux kernel 2.6.15.

5.1 Implementation Details

The programs for the PowerPC 970 were written in C using the AltiVec intrinsics [24]. We compiled all of the programs with the IBM XL C/C++ compiler for Linux v8. The programs for the Cell BE were also written in C using the intrinsics for SPE. We compiled our programs with the IBM XL C compiler for SPE. All of the programs used the memory with a 16 MB page size to reduce the overhead of TLB handling on both platforms.

In the implementations of AA-sort, we used half of the size of the L2 cache or local memory as the block size for the in-core sorting phase, 512 KB (128 K of 32-bit values) on the PowerPC 970MP and 128 KB (32 K of 32-bit values) on the SPE. The shrink factor for our vectorized combsort was 1.28. We discuss how to choose the parameters in the next section.

In our parallel implementation of the AA-sort, all of the threads first execute in-core sorting and then move onto the out-of-core merging phase after all of the blocks of input data are sorted. When executing the out-of-core merging phase with multiple threads, each thread executes independent merge operations as long as there are enough blocks to merge. In the last few stages, the number of blocks becomes smaller than the number of threads, and hence multiple threads must cooperate on one merge operation. Our implementation first divides one input stream into chunks of equal size for each thread, and then finds a corresponding starting point and finishing point for another input stream by executing binary search. Additionally, it executes rebalancing of the data among threads if the data size for each thread is not balanced [21].

To achieve the best performance on multicore processors, we employed implementation techniques to reduce the required bandwidth for system memory. The experimental implementations of the AA-sort used the 4-way merge. Our implementation of the bitonic merge sort for the Cell BE reduced the amount of data read from system memory by directly copying data from the local memory of another SPE core instead of from system memory whenever possible. This technique benefits from the huge bandwidth of the on-chip bus of the Cell BE. Those techniques do not change the computational complexity but they reduce the system memory bandwidth by changing the order of comparisons to improve memory locality.

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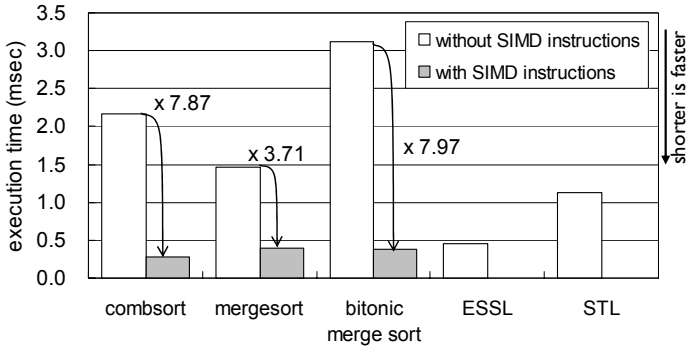

Fig. 10. Acceleration by SIMD instructions with our vectorization techniques for Combsort and Mergesort when sorting 16 K random integers on one PowerPC 970MP core.

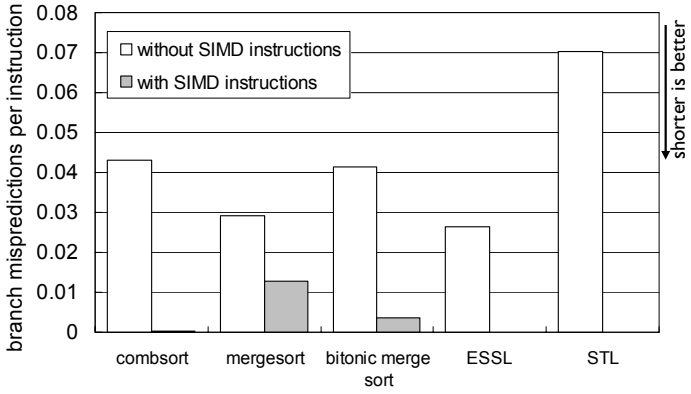

Fig. 11. Improvements in branch misprediction rate by using SIMD instructions.

5.2 Performance of Vectorized Combsort and Vectorized Mergesort

This section focuses on the performance of sequential implementations of each algorithm with primary emphasis on the effects of SIMD instructions. Then we discuss how to select the parameters including the block size and the shrink factor for in-core sorting. In this section, we separately evaluate the two algorithms used in the AA-sort, our vectorized combsort and our vectorized mergesort, to illustrate the effect of SIMD instructions for each algorithm. Note that the vectorized mergesort is not used with such small amounts of data when executing the entire AA-sort.

Fig. 10 compares the performance of the sorting algorithms for 16 K of random 32-bit integers using only one PowerPC 970MP core. All of the data to be sorted can fit into the L2 cache of the processor. The performance of our vectorized combsort, out-of-core algorithm, and the bitonic merge sort with SIMD instructions were drastically improved compared to the implementations without using the SIMD instructions, and the vectorized combsort achieved the highest performance among all of the algorithms tested.

The degrees of acceleration with the SIMD instructions for the vectorized combsort and the bitonic merge sort were larger than the degree of parallelism available with the SIMD instructions (4x) due to reduced number of branch mispredictions. Fig. 11 shows the branch misprediction rate measured by using a performance monitor counter of the processor. The branch misprediction rates were reduced by more than a factor of 10 for the combsort and the bitonic merge sort. The change of

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Table 2. Breakdown of Performance Gain

algorithm	speed up by SIMD	= reduction in instructions†	x improvement in CPI‡
combsort	7.87	4.06	1.94
mergesort	3.33	2.92	1.14
bitonic merge sort	7.97	4.69	1.70

† *reduction in instructions* = $instruction\_count_{scalar}$ / $instruction\_count_{SIMD}$
‡ *improvement in CPI* = CPI_{scalar} / CPI_{SIMD}

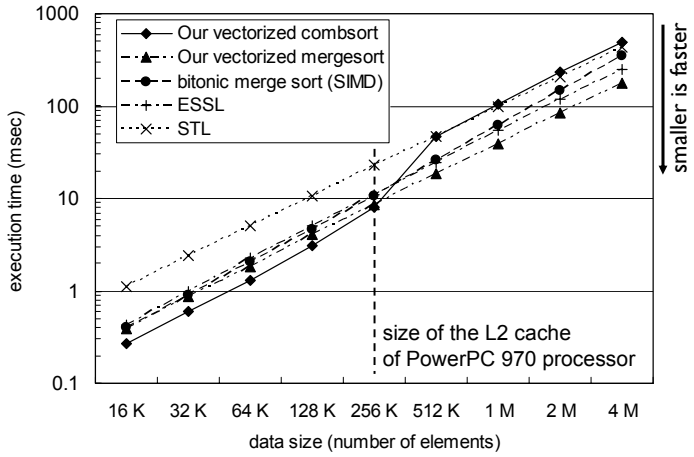

Fig. 12. Performance comparisons of our vectorized combsort and vectorized mergesort to other algorithms on one PowerPC 970MP core for sorting random 32-bit integers with various amounts of data.

misprediction rate was smaller for the mergesort because data-dependent conditional branches were reduced but not totally eliminated.

Table 2 shows a breakdown of the performance gain with SIMD instructions shown in Fig. 10 related to two factors: reductions in the numbers of instructions and improvements in cycles per instruction (CPI). The reductions in numbers of instructions were mainly due to the data parallelism of the SIMD instructions and the CPI improvements were due to the reduced branch overhead. For our vectorized combsort and bitonic merge sort, the numbers of instructions were reduced almost in proportion to the degree of data parallelism available from the SIMD instructions, while the reduction was not significant for the vectorized mergesort. This is because the vectorized merge operation for the vector registers shown in Fig. 6 is more complicated and requires more instructions than the naive merge operation for scalar values.

To determine the best value for the block size for PowerPC 970 processors, we evaluated the performance of the vectorized combsort and the vectorized mergesort with different amounts of data. Fig. 12 shows the relationship between the performances and the amounts of data. The x-axis shows the number of elements to be sorted and the y-axis shows the sorting time. Both axes are displayed as logarithmic scales. The figure shows that the vectorized combsort was the fastest for all amounts of data smaller than the size of the L2 cache. However its performance degraded drastically when the amount of data exceeded the L2 cache size and it was the slowest for larger amounts of data.

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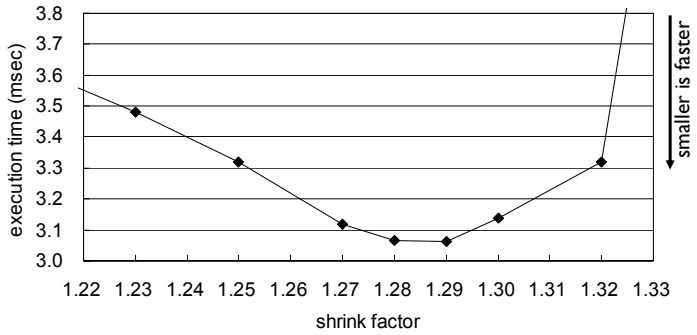

Fig. 13. Average execution time of sorting 128 K random integers by our vectorized combsort with different shrink factors.

This was due to the high cache miss ratio caused by a poor access locality in the combsort. For all amounts of data larger than the L2 cache size, the vectorized mergesort outperformed bitonic merge sort implemented with SIMD instructions, ESSL, and STL regardless of the amount of data. Based on this result we selected 128 K of 32-bit integers, or 512 KB, as the block size for the in-core sorting phase. This size corresponds to half of the size of the L2 cache of the processor.

Fig. 13 shows the average sorting time of a block of 128 K random 32-bit integers with the vectorized combsort with different values of the shrink factor. It achieved the fastest results when the shrink factor was 1.28 or 1.29. This result was almost consistent with the results for the original combsort by Lacey, the originator of the algorithm. The paper empirically showed that a shrink factor of around 1.3 gave the best results.

To quantitatively evaluate the benefit of using vectorized combsort for the in-core sorting phase, Fig. 14 compares the performance of each algorithm for sorting a block of 128 K integers of the five input datasets shown in the Table 3. Our vectorized combsort clearly outperformed other algorithms for all datasets. The advantages over the second best algorithm, our vectorized mergesort, were about 40%. The three algorithms using SIMD instructions, vectorized combsort, vectorized mergesort and the bitonic merge sort, showed much smaller dependencies on the input dataset than the other two algorithms. This is because they did not suffer from branch mispredictions even for random inputs. The performance of the ESSL and the STL were degraded severely in some cases. Our vectorized combsort may also show poor performance for some datasets, since it uses a heuristic approach. But we did not observe such significant degradations in those datasets we evaluated. Our vectorized mergesort does not show catastrophic performance even in the worst case.

From those results, we composed our AA-sort by combining the vectorized combsort for the in-core sorting and the vectorized mergesort for the out-of-core merging phase with the block size for in-core sorting of 128 K 32-bit integers, or 512 KB, and the shrink factor of 1.28 to achieve the best performance in sorting.

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Table 3. Description of Datasets.

dataset	description	pseudocode of initialization
A	uniform random	`for (i=0; i<N; i++) { data[i] = uniform_random(); }` // uniform random values in the range from 0 to 0xFFFFFFFF
B	Gaussian random	`for (i=0; i<N; i++) { data[i] = gaussian_random(); }` // Gaussian random values with standard deviation of 2^{24}
C	almost presorted	`for (i=1; i<N; i++) { data[i] = i; } data[0] = N;`
D	presorted (forward)	`for (i=0; i<N; i++) { data[i] = i; }`
E	presorted (reversed)	`for (i=0; i<N; i++) { data[i] = N-i; }`

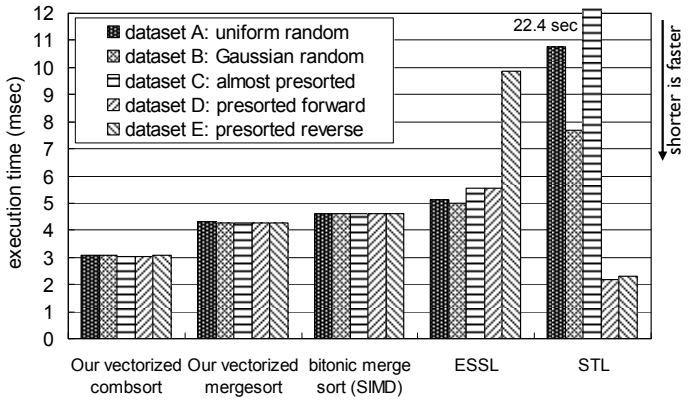

Fig. 14. Average execution time of sorting for various input datasets with 128 K integers on one PowerPC 970MP core.

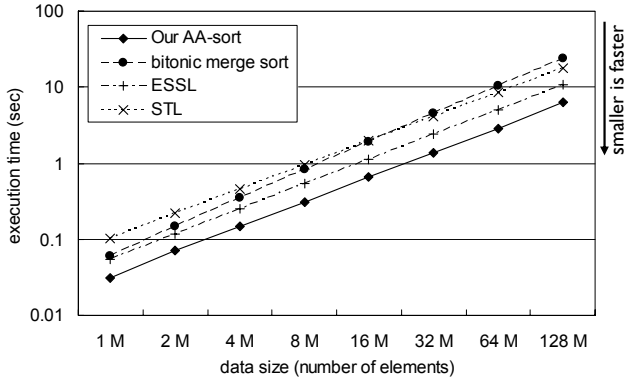

Fig. 15. Performance of sequential version of each algorithm on a PowerPC 970MP core for sorting uniform random 32-bit integers with various data sizes.

5.3 Performance for 32-bit Integers and Floating-Point Values

In this section, we discuss the performance of sorting for large 32-bit integer and floating-point arrays. Fig. 15 compares the performance of sequential versions of four algorithms to sort random 32-bit integers on the PowerPC 970MP. The AA-sort and the bitonic merge sort were implemented with SIMD instructions. The x-axis shows the number of elements up to 128 million elements (512 MB) and the y-axis shows the execution time. The AA-sort achieved the best result among all of the algorithms for all amounts of data. It was 1.8 times faster than the ESSL and 3.0 times faster than the STL when sorting 32 million integers. It also surpassed the performance of the bitonic merge sort by 3.3 times. The performance advantage of the AA-sort over the bitonic merge sort became larger with larger amounts of data because of the larger computational complexity of the bitonic merge sort.

Fig. 16 shows the execution time of parallel versions of the AA-sort and the bitonic merge sort on

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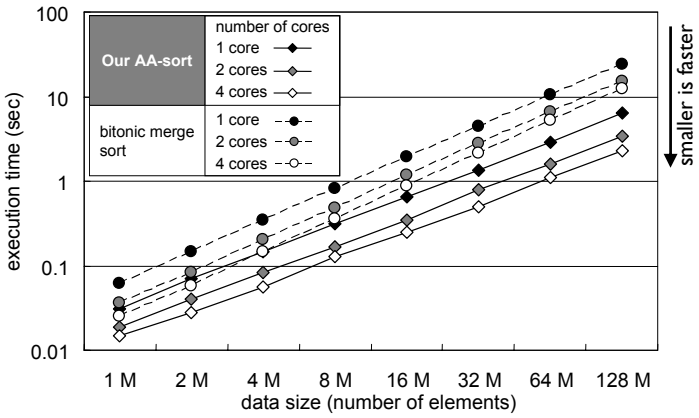

Fig. 16. Performance of parallel versions of our AA-sort and GPUTeraSort using up to 4 cores of PowerPC 970MP for sorting uniform random 32-bit integers with various data sizes.

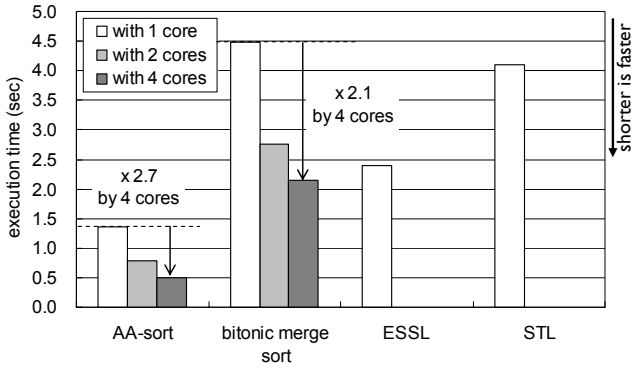

Fig. 17. The execution times of parallel versions of AA-sort and GPUTeraSort for sorting 32 million uniform random integers on up to 4 cores of PowerPC 970MP.

1, 2, and 4 PowerPC 970MP cores for various amount of uniform random integers. The results showed that both algorithms benefited from multiple cores and our AA-sort outperformed the bitonic merge sort regardless of the amount of data using the same number of cores.

Fig. 17 compares the speed ups by using multiple cores. It also shows the performance of the ESSL and the STL on only one core. The AA-sort achieved larger speed ups compared to bitonic merge sort. As a result, the performance of the AA-sort was 4.2 times higher than the performance of the bitonic merge sort when using 4 PowerPC 970MP cores. The better scalability of the AA-sort was because the bitonic merge sort has a higher communication/computation ratio than the AA-sort and the memory bandwidth was a bottleneck that limited the scalability.

Fig. 18 illustrates how the performance of each algorithm depends on the five input datasets described in Table 3 when sorting a block of 32 million integers using up to four cores of PowerPC 970MP. The results were consistent with the results for a smaller block that fitted into the L2 cache shown in the Fig. 14. The AA-sort and the bitonic merge sort implemented with SIMD instructions showed much smaller dependencies on the input dataset than the other two algorithms. The performance invariance of the AA-sort and the bitonic merge sort were unchanged even with the multiple cores.

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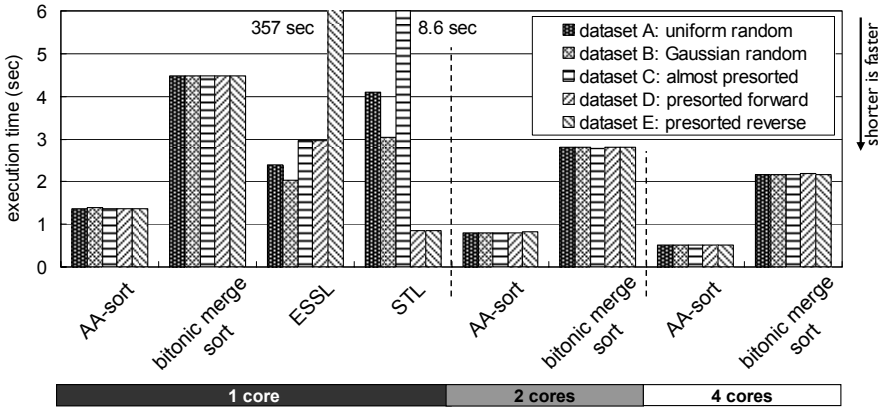

Fig. 18. Performance comparison for various input datasets with 32 million integers on up to four PowerPC 970MP cores.

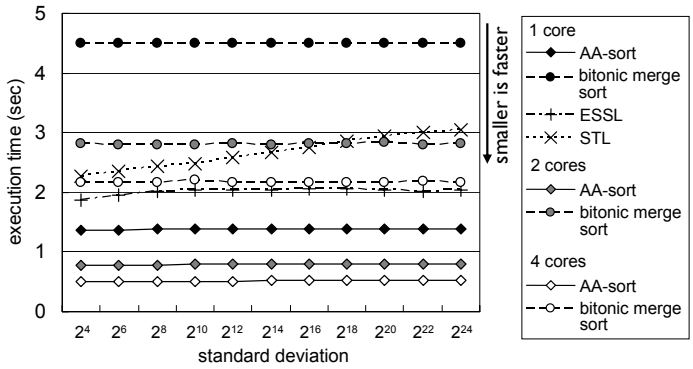

Fig. 19. The effect of the standard deviation on the performance of each algorithm when sorting 32 million Gaussian random integers.

Fig. 19 shows the sorting time for 32 million of Gaussian random integers with different standard deviations. The AA-sort and the bitonic merge sort showed almost constant sorting times regardless of the standard deviations of the input dataset. ESSL and STL achieved the fastest results with the smallest standard deviations. Even in the best case for those algorithms, the AA-sort outperformed ESSL by 36% and STL by 65% using only one core. Hereinafter, we use the uniform random values for the input datasets.

Fig. 20 compares the sorting time for 32 million uniform random 32-bit integers and 32-bit (single-precisions) floating point values. The AA-sort took 4.8% longer to sort the floating point values compared to the sorting of the same number of integers using one core. The performance difference between integers and floating-point values was much larger for the two scalar sorting algorithms, while it was only 0.4% for the bitonic merge sort. This is because floating-point values have longer compare-to-branch latency than integers for scalar comparisons on the PowerPC 970MP, while both data types have the same latency for vector comparisons. The bitonic merge sort uses only vector comparisons and hence its performance did not depend on the data type being sorted. The AA-sort uses scalar comparisons in addition to vector comparisons in the out-of-core merging phase, and thus its performance differs slightly for integers and floating-point values. The differences reduced with increasing number of cores because the system memory bandwidth limited the performance when using multiple cores and hence the effects of the longer instruction latency

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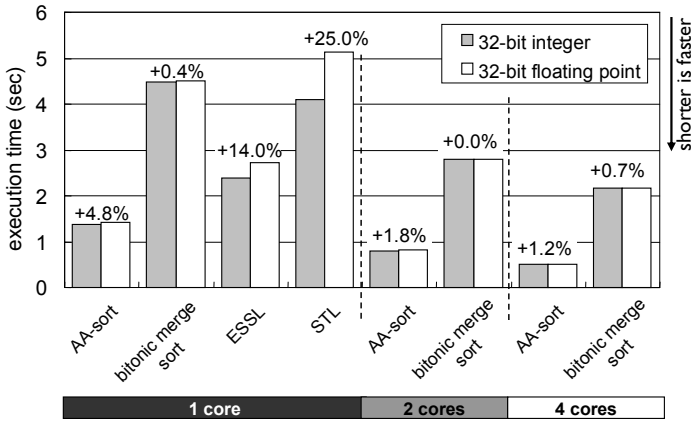

Fig. 20. Performance comparisons for 32-bit integer arrays and 32-bit floating point arrays with 32 million values using up to four cores of PowerPC 970MP.

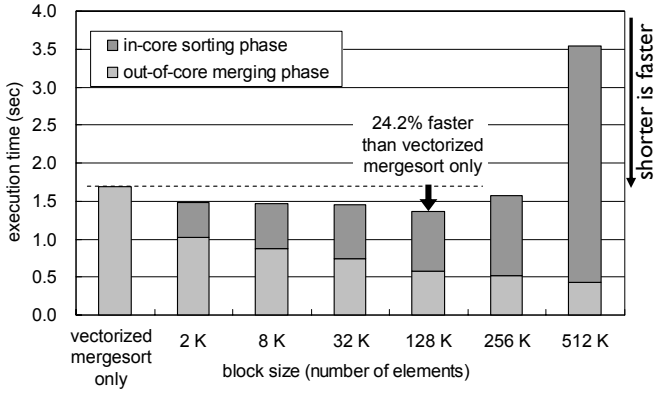

Fig. 21. Average execution time of sorting 32 million uniform random integers for AA-sort with different block size.

were less significant.

Fig. 21 shows how the block size for the in-core sorting phase affected the performance of the AA-sort when sorting 32 million uniform random integers using one PowerPC 970MP core. As shown in Fig. 14, the vectorized combsort was faster than the vectorized mergesort for in-core sorting and thus the larger block size brought the larger speed up while the size of a block was smaller than the size of the L2 cache of the processor, 256 K elements (or 1 MB). However, the block sizes larger than the size of the L2 cache drastically increased the execution time of the in-core sorting phase due to frequent L2 cache misses. Because we used 128 K elements as the block size, the AA-sort outperformed the vectorized mergesort by 24.2%.

Fig. 22 illustrates the execution time breakdown of the AA-sort into the in-core sorting phase and the out-of-core merging phase with various numbers of uniform random integers to sort. To show the importance of the in-core sorting phase, the figure also illustrates the relative performance of the vectorized mergesort. As discussed in Section 4, the computational complexity of the in-core sorting phase is $O(N \bullet \log(B))$, while that of the out-of-core merging phase is $O(N \bullet \log(N/B))$. Here, the block size, B, is a constant during the experiments. Hence the out-of-core merging phase consumed larger parts of the total execution time with larger amounts of data. However even with the largest amount of data we tested, 128 million 32-bit integers or 512 MB, more than half of the total execution time

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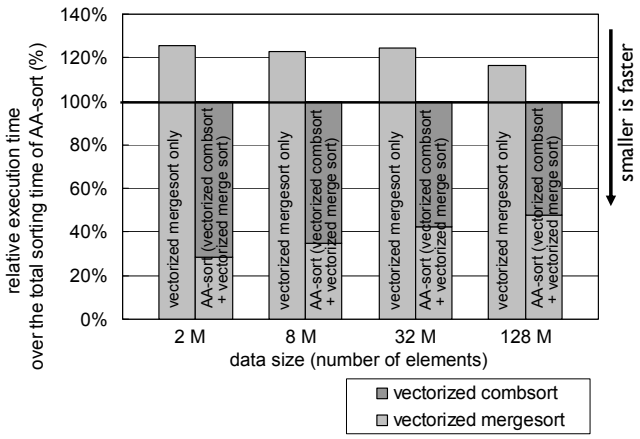

Fig. 22. Performance improvements by using the vectorized combsort for the in-core sorting phase over the sorting only using the vectorized mergesort on one PowerPC 970MP core.

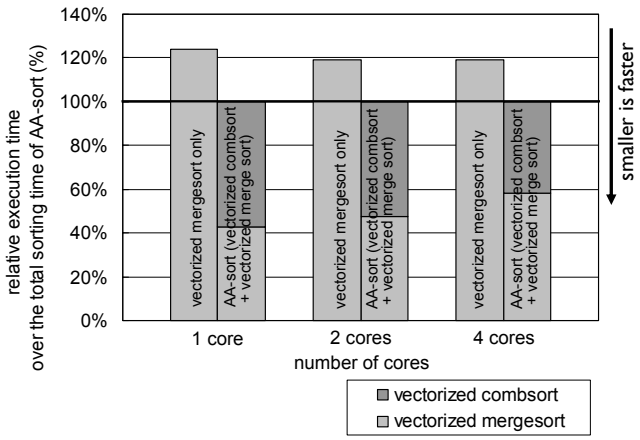

Fig. 23. Execution time breakdown of parallel version of AA-sort with 32 million uniform random integers on up to 4 cores of PowerPC 970MP.

was consumed by the in-core sorting phase and thus the performance of the in-core sorting phase mattered. The AA-sort improved the performance by up to 25.6% compared to the vectorized mergesort. Though the performance advantage of the AA-sort became smaller for larger data size, the benefit was still significant even for sorting 128 million integers.

By considering the computational complexity of the two phases, we can estimate the ratio in computation time in the AA-sort for much larger amount of data. For example, the in-core sorting phase still shares more than 40% of the total computation time for sorting 8 billion 32-bit integers, or 32 GB.

Fig. 23 shows the execution time breakdown of the AA-sort for sorting 32 million uniform random integers with up to 4 PowerPC 970MP cores. The fraction of execution time for the out-of-core merging phase increased with increasing numbers of processor cores. This was due to the poorer scalability of the out-of-core merging phase compared to the in-core sorting phase, which scaled almost linearly with number of cores. In the in-core sorting phase, most memory accesses were served by the L2 cache because this phase sorted blocks that fitted into the L2 cache. The out-of-core merging phase generated more L2 cache misses and hence the bandwidth to the system

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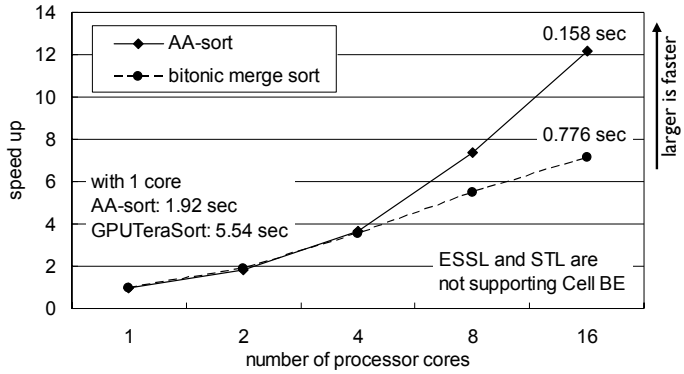

Fig. 24. Scalability with increasing number of cores on Cell BE for 32 million random integers.

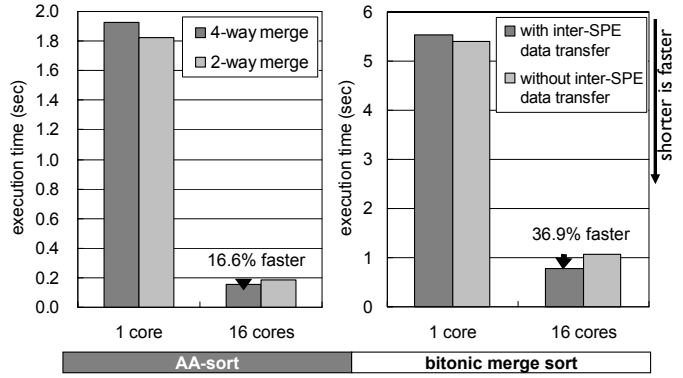

Fig. 25. Average execution time of sorting for 32 million random integers with and without techniques to reduce system memory bandwidth on Cell BE.

memory became a significant scalability bottleneck. Fig. 23 also shows the performance advantage of the AA-sort over the vectorized mergesort. The advantages were not significantly affected by the number of cores used.

To see the performance scalability with larger numbers of cores, Fig. 24 shows the scalability of the AA-sort and the bitonic merge sort on the Cell BE up to 16 cores when sorting 32 million 32-bit integers. Both algorithms showed almost linear speed up for up to 4 cores, since Cell BE provides more memory bandwidth than PowerPC 970MP. With more than 4 cores, our AA-sort demonstrated better scalability than the bitonic merge sort. For example, the AA-sort achieved a speed up of 12.2 for 16 cores while the bitonic merge sort achieved 7.1. This was because the bitonic merge sort has a higher communication/computation ratio than the AA-sort and the memory bandwidth was a bottleneck that limited the scalability. As a result, the performance of the AA-sort was better than the bitonic merge sort by 4.9 times with 16 Cell BE cores.

Our implementation of the AA-sort and bitonic merge sort used techniques to reduce the required system memory bandwidth as described in Section 5.2, the 4-way merge for the AA-sort and the inter-SPE data transfer for the bitonic merge sort. Fig. 25 depicts how those techniques affected the overall sorting performance. The techniques improved the performance when using 16 SPE cores by 16.6% for the AA-sort and by 36.9% for the bitonic merge sort while they degraded the performance using only one SPE core. This was because those techniques incurred additional computation overhead as a trade-off for reduced memory bandwidth and thus they did not improved the

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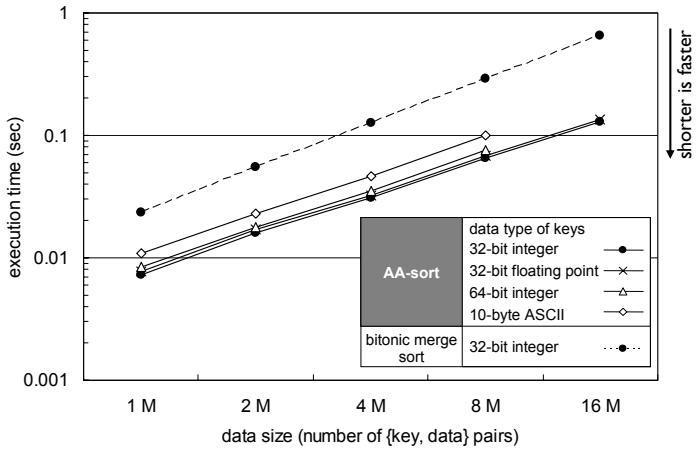

Fig. 26. Performance comparisons of the data type of the key for sorting {key, data} pairs on the Cell BE using 16 cores.

performance with small number of cores, where the memory access latency were totally hidden behind the computation by double buffering technique and thus the system memory bandwidth was not a limiting factor of the performance.

5.4 Performance for {Key, Data} Pairs

This section focuses on sorting for pairs of a key and associated data such as a pointer to the structure having that key value. Fig. 26 shows the sorting times of the AA-sort and the bitonic merge sort for sorting pairs with various data types for keys while using 16 Cell BE cores. The x-axis shows the number of elements up to 16 million pairs (128 MB). In the measurements the keys and the attached data are stored in distinct arrays. The tested data types of the keys included single-precision floating-point values, 64-bit integers, and 10-byte ASCII strings. The floating point keys and the integer keys were initialized using uniform random numbers. For the ASCII string keys, we used the input data generator of the Sort Benchmark (http://sortbenchmark.org/) to initialize the keys, and sorted them into order with the strnicmp() function.

Our implementations for wider keys, 64-bit integers and 10-byte ASCII strings, employed the hybrid approach of our algorithm and radixsort. Govindaraju *et al.* [15] also used a similar hybrid approach for the improved bitonic merge sort and radixsort in the bitonic merge sort. First it extracts the first few bytes from the keys and encodes them into 32-bit integer values, then sorts the pairs according to the encoded keys. After sorting by the first few bytes, when and only when multiple pairs have the same encoded keys, the pairs having the same encoded key are sorted using the next few bytes. The results shown in Fig. 26 include the time for key extraction and encoding. The input for our sorting function was pairs of {key, pointer}, and the output was a sorted array of pointers. The performance of the AA-sort for sorting 16 million pairs with random integer keys was about 1.6 times slower than that for sorting 16 million simple 32-bit integer values. However the AA-sort achieved up to 5.0 times faster results than the bitonic merge sort for the {key, pointer} pairs with 32-bit integer keys. For the wider keys, the performance was slightly degraded due to the overhead of the key encoding and repeated sorting. Even the slowest case with the AA-sort, for the keys of

10-byte ASCII strings, was much faster than the bitonic merge sort for the pairs with 32-bit integer keys.

6. CONCLUSION

This paper describes a new high-performance sorting algorithm that we call Aligned-Access sort (AA-sort). The AA-sort is suitable for exploiting both the SIMD instructions and thread-level parallelism available on today's multicore processors. The AA-sort does not involve any unaligned memory accesses that attenuate the benefit of SIMD instructions, and hence it can effectively exploit the SIMD instructions. We implemented and evaluated the AA-sort on PowerPC 970MP and Cell Broadband Engine processors. In summary, a sequential version of the AA-sort using SIMD instructions outperformed that of IBM's ESSL by 1.8 times and the bitonic merge sort using SIMD instructions by 3.3 times on the PowerPC 970MP when sorting 32 million random 32-bit integers. Also, a parallel version of the AA-sort demonstrated better scalability with increasing numbers of cores than a parallel version of the bitonic merge sort. The AA-sort achieved speed up of 12.2 for 16 cores on the Cell BE, while the bitonic merge sort achieved 7.1. As a result the AA-sort was 4.2 times faster on 4 PowerPC 970MP cores and 4.9 times faster on 16 Cell BE cores compared to the bitonic merge sort.

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