2016 IEEE 66th Electronic Components and Technology Conference

Toward high-yield 3D self-alignment of flip-chip assemblies via solder surface tension

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Flip-chip assembly with self-alignment down to sub-micron accuracy opens the door for low-cost assembly of micro-photonic chips. The surface tension of melted solder can be used to bring chips into alignment. The use of lithographically defined mechanical structures to stop the solder induced movement provides sub-micron alignment accuracy. However, several factors can impact the solder re-alignment yield. In this paper, we investigate the various yield limiting contributors and show that sensitivity to solder volume is the dominating factor. Variation in the amount of solder strongly impacts the lateral and vertical force induced by the solder, resulting in two small a process window for manufacturability. We show through models and experiments a design-based solution that dramatically improves the process window and yield. By the addition of local solder "reservoirs" we create a self-balanced system to improve solder plating tolerances from just a few percent to nearly a factor of two.

Introduction

Solder-induced alignment of opto-electronic chips has been pursued for two decades [1-4] but its broad application to manufacturing and its potential for low-cost assembly of micro-photonic components has yet to be realized. Our recent work has demonstrated flip-chip assembly with self-alignment down to sub-micron accuracy [5]. This level of performance is particularly useful in InP laser to Si photonic assemblies, where sub-micron alignment in three dimensions (3D) is required for low optical connection loss.

High accuracy alignment is provided by solder surface tension forces of purposefully offset solder pads, which re-align chips during solder reflow in belt ovens. Lithographically defined structures mechanically stopping the solder-induced motion provide the sub-micron alignment accuracy. While the details of our previous experiments are given in [5], figure 1 shows an overview of the features of our chips and substrates. Both have metallized pads, typically made of Nickel and Copper, and the substrates pads are covered by a thick layer of lead-free solder, typically Sn with a small percentage of silver. Vertical alignment is provided by vertical posts which are referred to as standoff, and are accurately defined by a lithographic and dry-etching process.

During solder reflow, solder melts and fully wets the metallized pads, bridging the gaps between the pads belonging to the substrate and the flipped chip. Figure 1 shows the solder induced lateral and vertical forces on the chip for a most ideal situation that leads to reliable chip motion. Chips move horizontally (in X and in Y directions) and slide on the standoffs until they butt against alignment stops lithographically defined on both sides of the assembly.

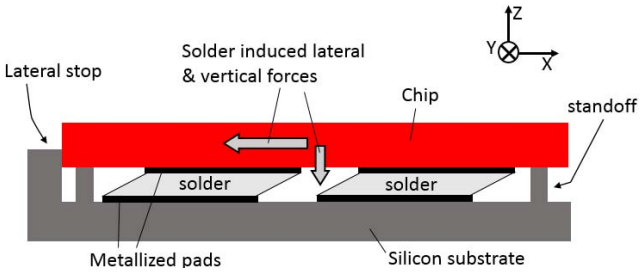

Figure 1. Configuration of chips and substrates for 3D self-alignment via melted solder.

Experimental observations on 1st generation designs

We have previously shown [5], through optical microscopy and cross-section SEMs, that deeply sub-micron alignment accuracy can be achieved. Our more recent demonstrations comprised several silicon-photonic circuits that include single-mode waveguides. We constructed two types of circuits:

- Si photonic substrate chips with lithographically defined standoffs and lateral stops meant to resemble CMOS-integrated photonic chips.
- Si-photonic flipped chips designed to resemble small optoelectronic elements such as III-V laser chips or semiconductor optical amplifiers (SOAs).

Figure 2 shows a view of few assembled chips, along with an IR picture through the chip of light scattering in

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DOI 10.1109/ECTC.2016.239

the waveguides, as it passes from the substrate to the flipped chip. Sub-micron alignment is key to the guiding of the light from one photonic circuit to another. Detailed description of the optical structures and of the light coupling results are presented elsewhere [6].

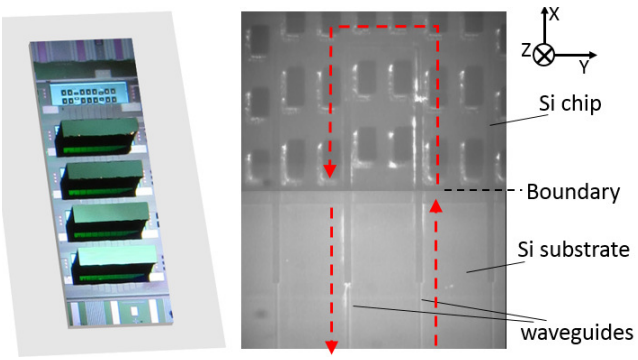

Figure 2. Left: Several Si-photonic flipped chips are mounted on a Si-photonic substrate circuit. Chips & substrate hold single-mode waveguides. One chip was left unmounted for illustration.
Right: IR microscopy of a region of the circuit on the left, with noticeable scattered IR along the light path. IR radiation is guided through butt-coupled waveguides from the substrate into the chip and back.

While we have shown the capability of this solder-induced self-alignment technique, we have also been able to identify some limitations. These appeared during our development work as challenges with re-alignment yield. While some chips were properly re-aligned others were not creating bleak prospects on the manufacturability of self-alignment. It is the object of this paper to present our understanding of the causes and to describe how we are overcoming them.

We have identified the following list of possible yield-limiting factors:

- Particulate contamination
- Friction or stiction at the mechanical alignment features
- Variation in plated solder height and/or standoff height
- Poor solder surface tension
- Gas pockets in the melted solder
- Solids phases or residues in melted solder
- Poor wetting of solder onto the metallic pads.

A first yield detractor in microelectronic is particulate contamination. Since our circuits involve micron size dimensions, especially for the gaps between alignment stops, it has become necessary to operate in a relatively clean environment. The fabrication of our test structures occurs in clean-room environment, and the preparation of the parts (cleaving or dicing) is followed by good cleaning practice as well as preparations and sorting under cleaned laminar air-flow. We have brought the level of dust and particle contaminates to a level low enough that it cannot explain the observed low yield.

A second yield detractor is friction or stiction at the mechanical alignment features, especially between the top of the standoffs and the chip surface. We conducted an experiment where we manually applied a few nano-liters of perfluorinated lubricant on top of the standoffs. We initially verified under microscope that the oil stays mostly put, and does not degrade under reflow temperature. The rest of the procedure was unchanged. The addition of oil translated to an immediate increase of the chip alignment yield by several fold. While the positive impact was encouraging, we needed deeper understanding of the cause of the excess friction. Through computational work, we have related the excess friction to incorrect balance between vertical and horizontal solder forces. This force balance is sensitive to variations in solder volume and standoff height.

While all factors require resolution for optimal yield, we did not find as much a contribution to yield from the other factors in the list above. We are focusing this paper on the impact of variations in the relative height of the solder and standoff.

Balance of vertical and horizontal forces

The force induced by the melted solder on the chip corresponds to the derivative of the thermodynamic free energy of the system with respect to chip position. It is dominated by reduction of the solder surface energy through minimization of the solder's surface area. Therefore, it has been mostly described as a capillary force, or surface tension force. The surface of the solder acts as a film that pulls the chip both in the lateral (X-Y) and vertical (Z) direction. A related approach to understanding the impact of surface tension is through the pressure it creates within the solder, which is dictated by the known Young-Laplace equation:

$$P = \gamma \left(\frac{1}{Rx} + \frac{1}{Ry} \right) \qquad (1)$$

where γ is the coefficient of surface tension and Rx and Ry are the principal radii of curvature. The resulting pressure within the liquid can induce a force Fz along the vertical (Z) direction that may be substantially larger

than would be obtained with a simple estimate of the surface tension force amounting to γ L (where L is the perimeter of the pad). Furthermore, because the radii of curvature can be either positive or negative (corresponding to a convex or concave surface), the pressure inside the liquid solder gains either a positive or a negative value. And therefore, the potentially large pressure force can be of either sign.

To better appraise the effect of the relative solder to standoff height on the vertical component of the solder force, Fz, it is instructive to compare the situations of chip alignment without standoffs and with standoff shown in Figure 3 and 4, respectively. The amount of solder is dictated by details of the electroplating process, used for depositing solder on the substrate metallized pads. A typical window of ± 10% in height variation is observed for a production plating process, accounting for variations across wafer and plating-bath parameters over time. An additional window (± 2 to 5% typ.) must be included to account for variations in standoff height and for pads metallization. Figure 3 and 4 highlight the effects of lack of solder (by under-plating) and of excess solder (by over-plating) on the lateral and vertical force. The situation without standoffs (fig.3) is amenable to chip alignment in 2-D only, in the X-Y plane. The chip essentially "floats" on the melted solder and the overall vertical force is zero, independent on the amount of solder. Furthermore, the lateral force is only marginally dependent on solder height.

The situation is very different in 3D alignment, with standoffs, shown in fig.4. In the case of a lack of solder, the vertical chip motion is constrained by the standoffs. The solder pulls in and its surface makes a concave-like shape. The radius of curvature can become small – down to half the chip-substrate spacing - which dictates a large negative pressure according to the Young-Laplace equation (1). This negative pressure induces a vertical downward pointing force which can be large compared to the lateral force and orders of magnitude larger than gravity. Hence, the chip can only move laterally if the coefficient of friction to the standoffs is correspondingly small, which explains the improved yield observed in our previous experiment with introduction of lubricant. On the other hand, excess solder produces a positive pressure which lifts the chip and creates a misalignment in the Z direction.

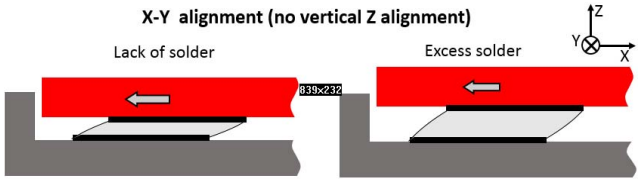

Figure 3. 2D (X-Y) alignment. In both cases of a deficiency or excess of solder material, the overall force by the melted solder on the chip is lateral, and there is no net vertical force.

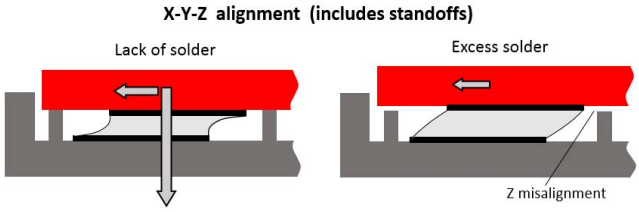

Figure 4. 3D (X-Y-Z) alignment. A lack of solder induces a substantial vertical force, an excess solder induces a vertical (Z) misalignment.

We created a model to better estimate the solder window that provides for a correct balance of forces: a vertical force pointing downward but also smaller than the lateral force to ensure lateral motion for typical coefficients of friction smaller than one. For simplicity, our model takes square solder pads with details shown on figure 5.

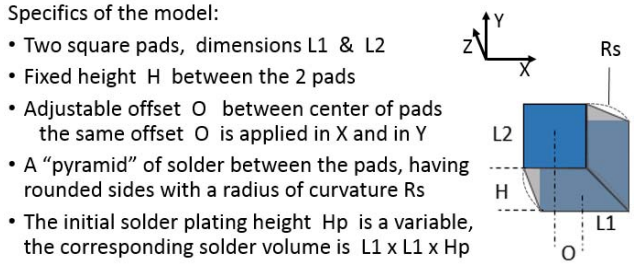

Figure 5. Three-dimensional model for calculation of vertical and lateral solder forces.

The perfect pyramidal solder shape is an approximation of the real shape, albeit a not too distorted approximation. The lack or excess of solder is modeled as a rounding of the pyramid sides, with a calculated radius of curvature Rs depicted on fig.5 for each of the 4 sides. This simplifies the calculation while intuitively following the evolution of the solder shape as a function of the solder volume. Knowing Rs, the solder surface S is determined as the surface of the 4

sides of the pyramid. The lateral and vertical forces are then obtained from the 2 relations:

$$Fx = \gamma \, dS/dx$$

$$Fz = \gamma \, dS/dz$$

where the derivatives dS/dx and dS/dz are calculated as small changes in S when a small offset change dx or a small height change dz is applied. For coefficient of surface tension γ of the melted solder, we chose a value of 0.53 N/m [7].

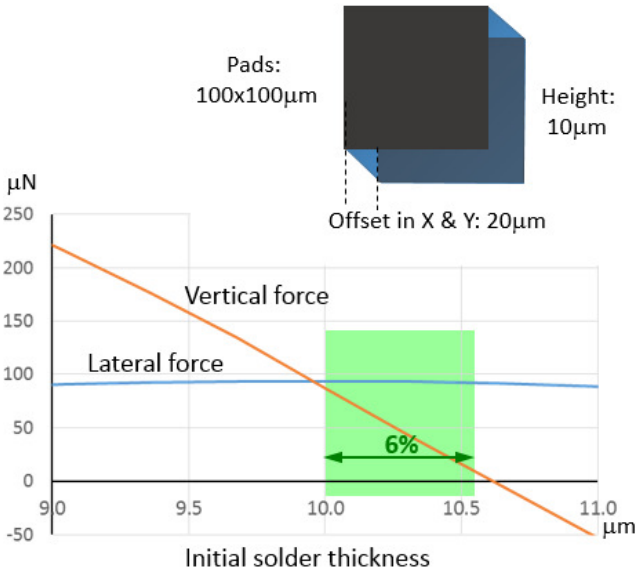

Figure 6. Calculated vertical and lateral solder forces for a typical solder pad geometry.

Results of the calculation for our typical solder pad geometry are given on figure 6. The graph displays the vertical and lateral forces as a function of initial thickness. Pads are assumed to be square, 100 um in width, offset by 20 micron in X and Y, and with a fixed gap in Z of 10 micron. The graph displays the vertical and lateral force as a function of initial thickness on the bottom pad, over the range between 9 and 11 micron (this range also accounts for other effects, including standoff height variation). While the lateral force displays a relatively constant value near 100 micro-Newton, the vertical force decreases strongly over the range of the calculations. A green area highlights the region where the vertical force has an acceptable value: it is both positive (indicative of an attractive force) and lower than the lateral force (allowing lateral chip movement). This window of acceptable solder thickness is only about 6%, and highlight the smallness of the tolerance window in solder plating and standoff height. Any assembly with solder thickness falling outside of this narrow window will not re-align properly exposing stark challenges to the manufacturability of solder re-alignment.

Experimental data and design-based solution.

To substantiate the validity of our model and our choice for γ = 0.53N/m, as well as to verify the shape and magnitude of the calculated forces, we built a mesa-scale model with the cantilever-based set-up described in figure 7, capable of measuring the vertical solder force at high temperature (250C), in a controlled atmosphere of nitrogen with a few percent of formic-acid vapor to reduce surface oxides that can prevent standard SnAg solder from flowing, and with a variable pad spacing. Cantilever material is beryllium copper, with length, width and thickness respectively equal to 14.8, 5.1 and 0.203 mm. Calculated stiffness is 504 N/m, close to the measured value of 499 N/m. The cantilever motion is measured via laser beam deflection.

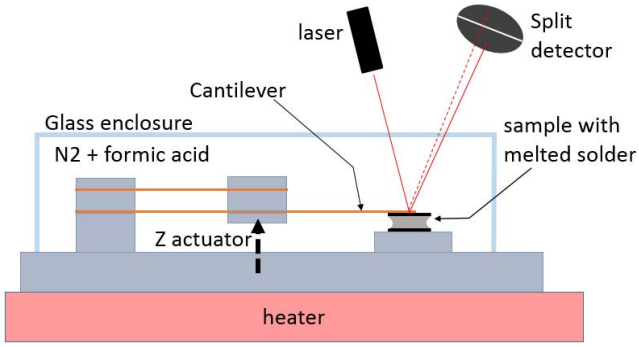

Figure 7. Experimental set-up for the measurement of vertical force of melted solder, as a function of spacing.

Figure 8 displays our measurement results for 3 different samples. Overlaid in dotted lines are calculated vertical forces. The agreement for both the magnitude and the trend is very reasonable, and confirms the validity of our model. This also confirms our value for γ and that our solder surface tension matches previously measured values [7].

The curves in figure 8 also highlight a key trend that instructs our new designs. Fully overlapping pads generate a strong vertical force and force gradient, whereas non-overlapping pads generate a weaker vertical force and force gradient. This observation is key for minimizing the variability of the vertical force as a function of relative solder to standoff thickness. The

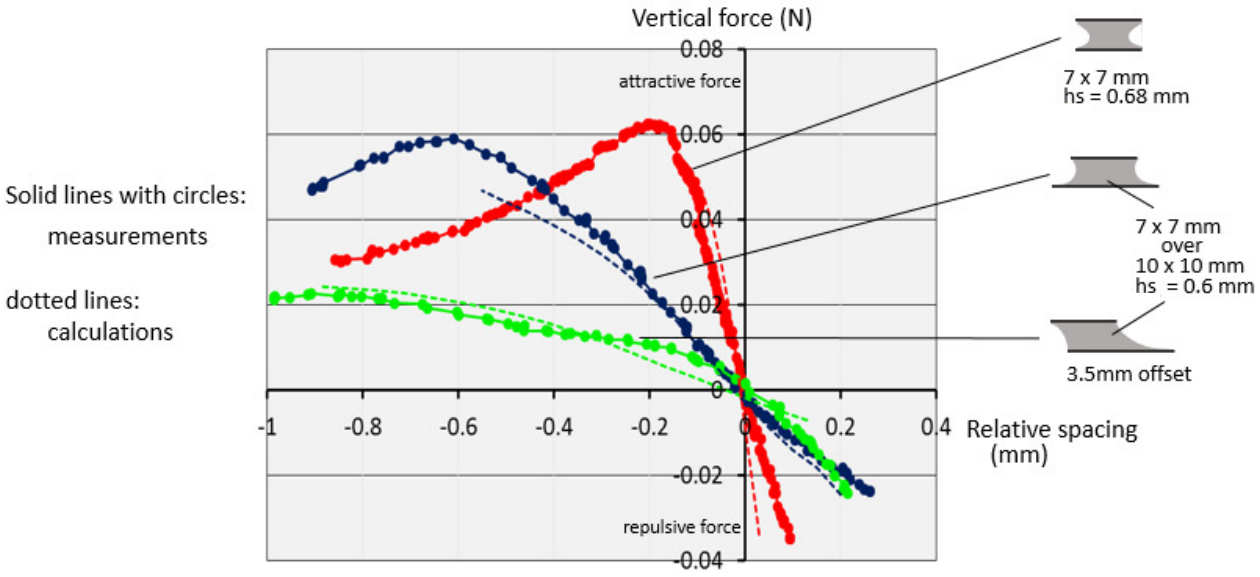

Figure 8. Vertical solder force as a function of vertical solder spacing.
Samples with tightly overlapping pads (red) yield large vertical force and force gradient.
Sample with non-overlapping pad regions (green) yield small vertical force and force gradient.

new designs include an area of solder that can breathe and change in volume without directly impacting the vertical force. This area of solder can be described as a reservoir of solder that can compensate for variations in relative solder to standoff thickness.

We have designed several types of solder reservoirs, including separate reservoirs, where a conduit connects a pad to a separate reservoir area. We have added this feature to our model, were a circular reservoir (a circular pad, with plated solder, having no corresponding chip pad) is connected with a small channel to a sample pad. Figure 9 and 10 display the calculated forces for 2 geometries: with integrated reservoir, consisting in a larger substrate pad, fig.9; and with separated reservoir, fig.10. In both cases, the acceptable range for the vertical force – highlighted in green – is very large and covers an approximate 2x range. The new designs confer a huge improvement to

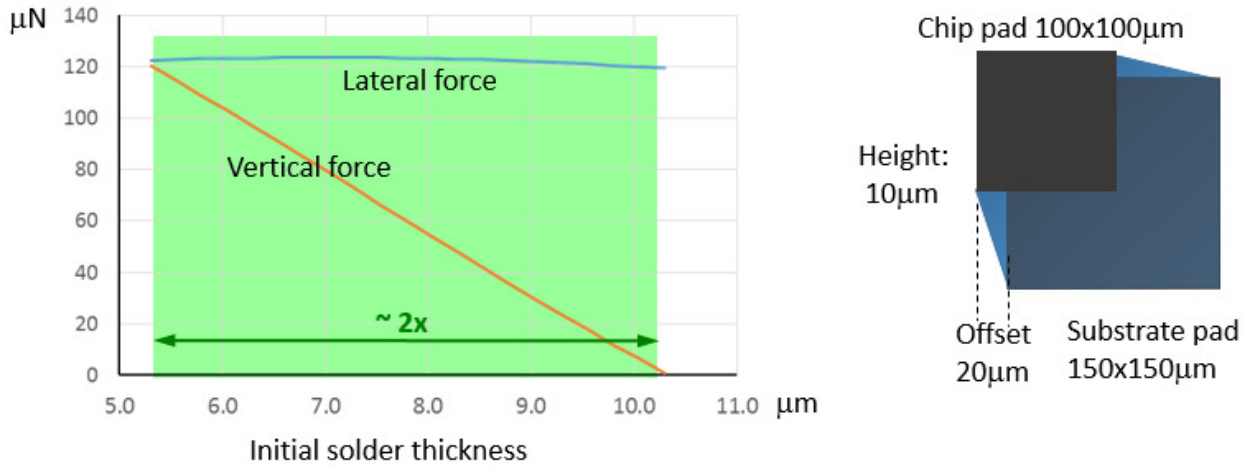

Figure 9. Calculated solder forces for solder pads with "integrated reservoir". The large area of non-overlapping pads serves as an adjunct reservoir of solder upon melting. Excess solder, due to over-plating, adds primarily to the reservoir. Lack of solder, due to under-plating, will be supplied from the reservoir. Consequently, the hydrostatic pressure in the liquid solder – and hence the induced vertical force – is less dependent on the initial amount of solder, and the process window (highlighted in green) is greatly improved.

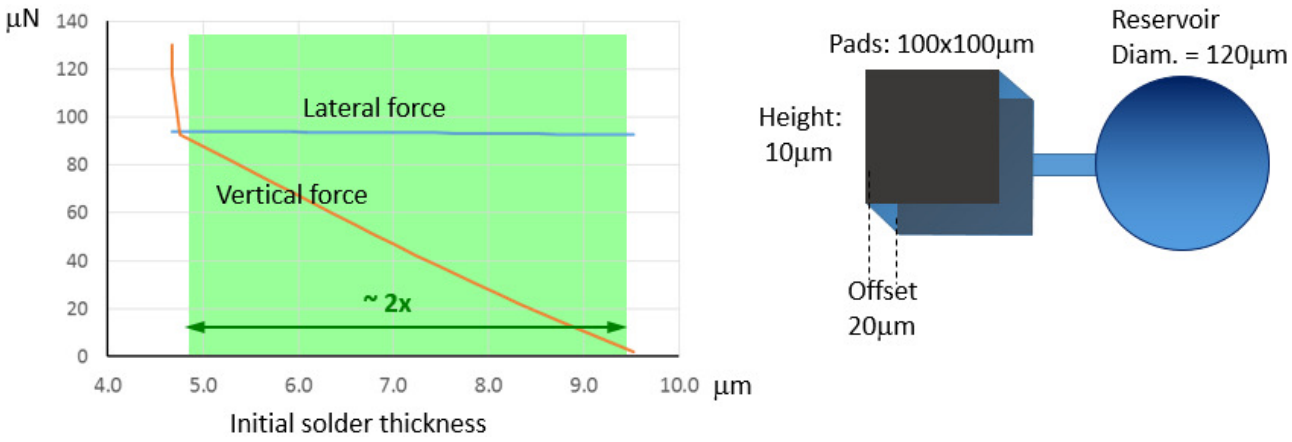

Figure 10. Calculated solder forces for solder pads with external reservoir. A small metallized line connects the bottom substrate pad to the reservoir pad and acts as a solder conduit. Excess (or lack) of solder primarily fills in (or empties) the reservoir. The process window is similar to the one in fig.9. Of notice is the left-most portion of the vertical force curve which rises suddenly, and serves as an indication that the reservoir of solder has become empty.

the process windows for both solder and standoff heights.

We have started to implement the new designs into newly fabricated chips and substrates. Figure 11 shows a composite picture (visible + IR) of an aligned chip on substrate. Our early results, with no lubricating oil and no selection of solder height to match standoff height, indicates that the design meets the objectives. Further tests on multiple chip builds are in process to statistically confirm the yield increase.

Conclusion

Understanding the impact of the variability of relative height, solder to standoff, on solder-induced forces was key to explain the low yield in chip self-alignment. New designs substantially relax the fabrication process tolerances for solder and standoff height, and appear to substantially increase the alignment success.

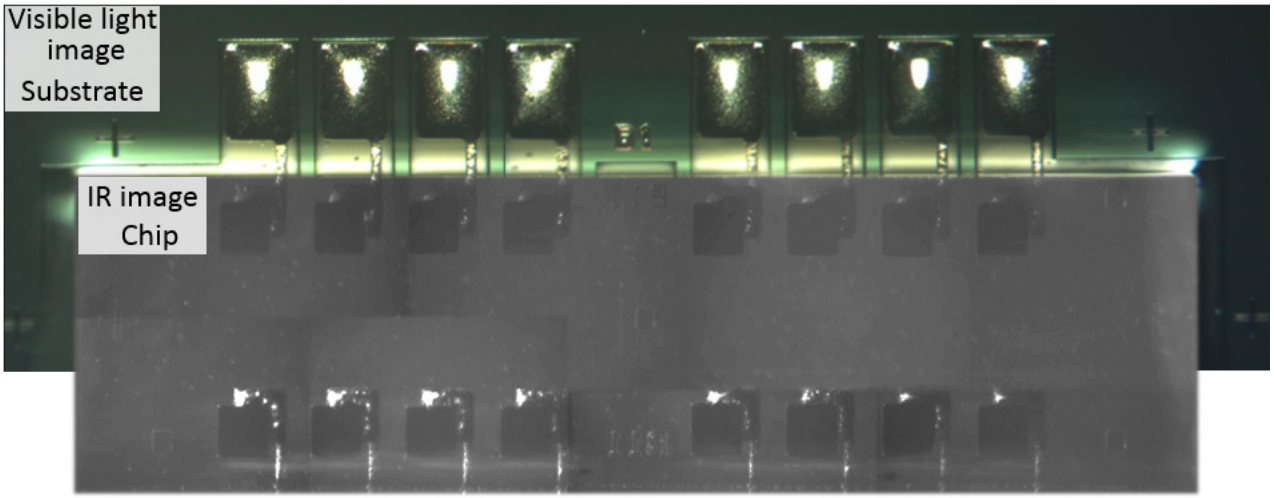

Figure 11. Composite image of a chip aligned over a substrate having pads with external reservoirs. Substrate and chip pads are square and appear in the IR image, being observed through the Si chip. Reservoirs belonging to the substrate are rectangular. They appear in the top part of the visible-light image. Visible and infra-red micrographs were assembled for clarity.

Acknowledgments

We would like to thank the staff of the Microelectronics Research Laboratory (MRL) at the IBM T.J. Watson Research Center where the photonic chips were fabricated. We would like to acknowledge the leadership from the managerial team in our organization, and in particular the insight and support from Yurii Vlasov, Wilfried Haensch, and William Green.

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