- **Jason Zebchuk**
  - **Title:** Reducing the Fixed-Costs of Directory-based Cache Coherence
  - **Abstract:** Cache coherence protocols are a necessary evil for most chip multiprocessors. While they provide a convenient, easy-to-use mechanism to support the ubiquitous shared memory programming paradigm, they incur area, energy, and latency overheads. Ironically, the same paradigm that makes cache coherence necessary also teaches that it should be avoided as much as possible. The search for performance inevitably leads to minimizing the amount of data communicated between processing cores, and this in turn reduces the number of times when cache coherence is actually necessary. However, while programmers might successfully reduce a program's dependence on the cache coherence protocol, they cannot eliminate all the overheads associated with coherence.

    Even when little data is being actively shared, the cache coherence protocol incurs some fixed costs to guarantee that it can maintain coherence at all times. For directory coherence protocols, one unavoidable, fixed cost, comes from the on-chip area dedicated to the coherence directory, and the energy required to access it. Even if the coherence protocol were to be turned off and the directory powered down to eliminate any leakage power, the area devoted to that structure cannot be reclaimed. This talk will examine two approaches to reducing these fixed costs associated with directory coherence protocols. First, the Tagless Coherence Directory uses Bloom filters to provide a scalable coherence directory. The second approach goes further and attempts to all but eliminate the need for a dedicated on-chip directory structure by instead multi-purposing the cache memories already available on-chip.
  - **Bio:** Jason Zebchuk has been a student at the University of Toronto since 2000. First, he completed the Engineering Science program with a focus on Computer Engineering, receiving his Bachelor of Applied Science in 2005. In 2007 he received a Master of Applied Science for his thesis entitled "RegionTracker: A Framework for Coarse-Grain Optimization in the On-Chip Memory Hierarchy." Since then, he has been researching memory hierarchies and cache coherence for large chip-multiprocessors in pursuit of a PhD. Since 2005, Jason has been studying under the supervision of Professor Andreas Moshovos, and his graduate studies have been supported by a Canadian Graduate Scholarship and a Postgraduate Scholarship from the Natural Sciences and Engineering Research Council of Canada.