- **Arun Raman**
  - **Title:** Speculative Parallelization using Software Multithreaded Transactions
  - **Abstract:** With the right techniques, multicore architectures may be able to continue the exponential performance trend that elevated the performance of applications of all types for decades. While many scientific programs can be parallelized without speculative techniques, speculative parallelism appears to be the key to continuing this trend for general-purpose applications. Recently-proposed code parallelization techniques, such as Speculative Decoupled Software Pipelining (Spec-DSWP), demonstrate scalable performance on multiple cores by using speculation to divide code into atomic units (transactions) that span multiple threads in order to expose data parallelism. Unfortunately, most software and hardware Thread-Level Speculation (TLS) memory systems and transactional memories are not sufficient because they only support single-threaded atomic units. This work proposes a Software Multithreaded Transaction (SMTX) system that enables techniques like Spec-DSWP on commodity multicore machines. The SMTX system yields a geomean speedup of 15x on a shared-memory multiprocessor with four 6-core processors (24 cores in total) running speculatively parallelized applications drawn mostly from the SPEC CPU benchmark suites. The SMTX system is designed to mitigate the costs of inter-core communication allowing it to be deployed on clusters that have much higher communication costs than multicore chips. On a 4-core 32-node (128 cores in total) cluster without shared memory, the SMTX system achieves a geomean speedup of 49x on the same application suite without any modifications to the application source code for clusters.
  - **Bio:** Arun Raman is a PhD candidate at Princeton University, and is a member of the Liberty Research Group headed by Prof. David I. August. He is primarily interested in making sense of the "multicore revolution". To this end, he is developing tools that will enable programmers to exploit multicore hardware with minimal effort. Arun is a founding member of the Computer Architecture Reading Group at Princeton, and an organizing committee member of the first Computer Architecture Day at Princeton (2009). He is an Intel Graduate Fellowship (2010-11) and a Princeton University Graduate Fellowship (2006-07) awardee. His teaching has been recognized by Princeton through an Outstanding Teaching Recognition award (2007). Arun received a master's degree in Electrical Engineering from Princeton University (2008), and a bachelor's degree in Electrical Engineering (2006) from the Indian Institute of Technology Roorkee.