- **Ulya Karpuzcu**
  - **Title:** Pushing Back the Many-core PowerWall
  - **Abstract:** Many-core scaling now faces a power wall. The gap between the number of cores that fit on a die and the number that can operate simultaneously under the power budget is increasing with technology scaling. In future designs, some of the cores may have to be dormant at any given time to meet the power budget. In this talk, I will cover two approaches to push back the many-cover power wall. The first approach relies on what we call Dynamic Voltage Scaling for Aging Management (DVSAM)—a new scheme for managing processor aging to attain higher performance or lower power consumption. In addition, I will introduce the BubbleWrap many-core, a novel architecture that makes extensive use of DVSAM. BubbleWrap identifies the most powerefficient set of cores in a variation-affected chip—the largest set that can be simultaneously powered-on—and designates them as Throughput cores dedicated to parallel-section execution. The rest of the cores are designated as Expendable and are dedicated to accelerating sequential sections. BubbleWrap attains maximum sequential acceleration by sacrificing Expendable cores one at a time, running them at elevated supply voltage for a significantly shorter service life each, until they completely wear-out and are discarded—figuratively, as if popping bubbles in bubble wrap that protects Throughput cores. In simulated 32-core chips, BubbleWrap provides substantial improvements over a plain chip. I will then continue with Near-Threshold Voltage Computing (NTC), where the supply voltage is only slightly higher than the transistors' threshold voltage. Unfortunately, a key NTC shortcoming is the higher sensitivity to process variations, which results in conservative designs. Moreover, past proposals to mitigate variation, such as variants of adaptive supply voltage, are unusable because, at NTC, the ability to tune the voltage practically vanishes. I will introduce a model of process variations at NTC, followed by a many-core architecture called CheckerBoard and its core-scheduling algorithmthat are designed to exploit process variations at NTC with simple hardware. This architecture uses a fixed voltage, and assigns its compute clusters to jobs based on the clusters' variation profiles and the application's characteristics. Our results show that process variations at 11nm have a larger impact in an NTC environment than in a conventional one.
  - **Bio:** Ulya R. Karpuzcu received the B.S. degree in electronics and telecommunication engineering, the B.S. degree in computer engineering (double major) from Istanbul Technical University, Turkiye, and the M.S. degree in electrical and computer engineering from University of Illinois, Urbana-Champaign. She is currently working toward the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign. Her research interests include impact of technology on (micro)architecture, energy-efficient many-core (micro)architectures and near-threshold computing. Ulya R. Karpuzcu received the Fulbright Fellowship in 2006, and the best paper award at MICRO'09 for the BubbleWrap paper.