- **Greg Gibeling**
  - **Title:** RePar: Reconfigurable Parallel Computing New Abstractions and Tools for Productivity and Performance
  - **Abstract:** Through the use of a novel representation, called Dataflow Stencil (DS), for computing applications we can combine ideas from reconfigurable and parallel computing with high productivity programming. This in turn enabled the creation of a Solution Compiler (SC), capable of synthesizing simple high level descriptions into high performance, parallel implementations on hardware platforms ranging from FPGAs to CPUs, andcombinations in between.
  - **Bio:** I am currently a 5th year PhD student in EECS at U.C. Berkeley. I am currently working on GateLib: a library for hardware and software research, and RePar: new abstractions and tools for productivity and performance in reconfigurable parallel computing. The goal of the RePar project is to explore tools and algorithms for synthesizing high quality hybrid systems from high level application descriptions. GateLib provides a necessary foundation for generating and testing this work, and is shared with a number of other projects.